BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

YELAHANKA – BANGALORE - 64

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE FILE

Semester: **I**

Course Code: **18ELN14**

Course Name: **Basic Electronics**

Course Faculty: Dr. Surekha Gondkar
Mrs. Chandraprabha R
Dr. Vijayalakshmi G V

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BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

Avalahalli, Doddaballapur Road, Yelahanka, Bangalore - 560064

Institution Calender of Events (CoE) 2020-21 (ODD Semester)

VISION OF THE INSTITUTE	To emerge as one of the finest technical institutions of higher learning, to develop engineering professionals who are technically competent, ethical and environment friendly for betterment of the society.
MISSION OF THE INSTITUTE	Accomplish stimulating learning environment through high quality academic instruction, innovation and industry-institute interface.

Month	Week	Sun	Mon	Tue	Wed	Thu	Fri	Sat	Working Days	EVENTS
September	W-1			1	2	3	4	5	5	1-Sept.: Commencement of B.E (III, V, & VII Sem.), MCA (III & V Sem.) & M.Tech (III Sem.) Classes
	W-2	6	7	8	9	10	11	12	6	10-Sept.: FYP/PBL Group Formation
	W-3	13	14	15	16	17	18	19	5	17-Sept.: Mahalaya Amavasya
	W-4	20	21	22	23	24	25	26	6	21-Sept.: FYP/PBL Guide Allotment; 21-Sept.: FIMS Update
	W-5	27	28	29	30				3	30-Sept.: FYP/PBL Synopsis Submission
October	W-6					1	2	3	2	2-Oct.: Gandhi Jayanthi
	W-7	4	5	6	7	8	9	10	6	5-7 Oct.: Internal Assessment (IA) Test - 1 B.E (III, V, & VII Sem.) M.Tech (III Sem.), MCA (III & V Sem.)
	W-8	11	12	13	14	15	16	17	6	14-Oct.: SMS Dispatch for IA-1; 16-17 Oct.: Students Feedback -1 on Faculty; 17-Oct.: PTA for Higher Semester
	W-9	18	19	20	21	22	23	24	6	20-Oct.: FIMS Update
	W-10	25	26	27	28	29	30	31	3	26-Oct.: Vijayadashami; 27-28 Oct.: FYP/PBL Patentability Review - 1; 30-Oct.: Eid Milad; 31-Oct.: Valmiki Jayanthi
November	W-11	1	2	3	4	5	6	7	6	1-Nov.: Kannada Rajyotsava; 5-7 Nov.:Internal Assessment (IA) Test - 2 B.E (III, V, & VII Sem.) M.Tech (III Sem.), MCA (III & V Sem.)
	W-12	8	9	10	11	12	13	14	6	14-Nov.: Tech-Transform 2020 Notification; 14-Nov.: SMS Dispatch for IA-2
	W-13	15	16	17	18	19	20	21	5	16-Nov.: Balipadyami Deepavali; 16-17 Nov.: Students Feedback - 2 on Faculty; 20-Nov.: PBL Patentability Review - 2/BMSIT Open Day; 20-Nov.: FIMS Update; 21-Nov.: Tech-Transfrom 2020
	W-14	22	23	24	25	26	27	28	6	27-28 Nov.: FYP Patentability Review - 2
	W-15	29	30						1	
December	W-16			1	2	3	4	5	4	3-Dec.: Kanakadasa Jayanti
	W-17	6	7	8	9	10	11	12	6	7-9 Dec.: Internal Assessment (IA) Test -3 B.E (III, V, & VII Sem.) M.Tech (III Sem.), MCA (III & V Sem.)
	W-18	13	14	15	16	17	18	19	4	16-Dec.: SMS Dispatch for IA-3; 17-Dec.: Last Working Day for B.E (3rd, 5th, & 7th Sem.), MCA (3rd & 5th Sem.) & M.Tech (3rd Sem.) Classes
	W-19	20	21	22	23	24	25	26		21-Dec.: FIMS Update; 25-Dec.: Christmas
	W-20	27	28	29	30	31				
	Total Number of Working Days								86	

CONTINUOUS INTERNAL EVALUATION

COURSE	SEM	START	END
INTERNAL ASSESSMENT - 1			
B.E	I	TBA	TBA
B.E	III, V, VII	05-Oct	07-Oct
MCA	III & V	05-Oct	07-Oct
M.Tech	I	TBA	TBA
MCA	I	TBA	TBA
INTERNAL ASSESSMENT - 2			
B.E	I	TBA	TBA
B.E	III, V, VII	05-Nov	07-Nov
MCA	III & V	05-Nov	07-Nov
M.Tech	I	TBA	TBA
MCA	I	TBA	TBA
INTERNAL ASSESSMENT - 3			
B.E	I	TBA	TBA
B.E	III, V, VII	07-Dec	09-Dec
MCA	III & V	07-Dec	09-Dec
M.Tech	I	TBA	TBA
MCA	I	TBA	TBA

SEMESTER END EXAMINATIONS

COURSE	START OF EXAM	END OF EXAM
B.E : I - SEM		
B.E : III, V, & VII - SEM	04-01-2021	23-01-2021
M.Tech: I - SEM		
M.Tech: III - SEM	04-01-2021	23-01-2021
MCA: I - SEM		
MCA: III & V - SEM	04-01-2021	23-01-2021

PROFESSIONAL TRAINING/INTERNSHIP VIVA-VOCE

COURSE	SEM	START	END
B.E			
M.Tech	III	25-Jan	08-Feb
MCA			

COMMENCEMENT OF EVEN SEMESTER (2020-21)

COURSE	SEM	DATE
B.E	III, V & VII	08-Feb
MCA	III & V	08-Feb
M.Tech	III	22-Feb

LIST OF HOLIDAYS

17-Sep	Mahalaya Amavasya
02-Oct	Mahatma Gandhi Jayanthi
26-Oct	Vijayadashami
30-Oct	Eid-Milad
31-Oct	Maharishi Valmiki Jayanti
01-Nov	Kannada Rajyotsava
16-Nov	Balipadyami Deepavali
03-Dec	Kanakadasa Jayanti
25-Dec	Christmas

PARENTS-TEACHERS ASSOCIATION

PTA	DATE
PTA - 1	17-Oct
PTA - 2	TBA

PRACTICAL EXAMINATION

COURSE	SEM	DATES
B.E	III, V, & VII	21-Dec to 31-Dec
MCA	III & V	21-Dec to 31-Dec
M.Tech	III	21-Dec to 31-Dec

ABBREVIATIONS

IA	Internal Assessment	FIMS	Faculty Information Mgmt. System
IIC	Institution Innovation Council	FYP	Final Year Project
PTA	Parents-Teachers-Association	PBL	Projects Based Learning

Hatha 4/9/2020
Coordinator - COE

Head - IQAC

PRINCIPAL

BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

YELAHANKA – BANGALORE - 64

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE NAME: BASIC ELECTRONICS

COURSE CODE: 18ELN14/24

COURSE OUTCOMES

1. Understand the operation of semiconductor devices and circuits.
2. Apply the knowledge of basics of semiconductor devices to build electronic circuits.
3. Analyse the working of analog and digital circuits for any application.
4. Design electronic systems using analog and digital devices.
5. Design and demonstrate(Hardware/simulation) the basic applications of electronic circuits in a team.

CO-PO MAPPING EXPLANATION

CO	Explanation
CO2	Strongly related to PO1 because the students can be able to Identify and comprehend the concepts of semiconductor devices and construct the circuits with the application of basic mathematics and science.
CO3	Strongly related to PO2 because the students can able to Analyse the working of analog and digital circuits for any real tine applications of the society
CO4	Strongly related to PO3 because the students can able design and enumerate the working principles of electronic systems.
CO5	Strongly related to PO5 and PO9 because the students can able design and conduct with the aid of standard modern tools in a team. Lightly related to PO10 as the students present the technical report in a team

BASIC ELECTRONICS

Semester	**: I/II**	**CIE Marks**	**: 40**
Course Code	**: 18ELN14/24**	**SEE Marks**	**: 60**
Teaching Hours/week (L:T:P)	**: 2:2:0**	**Exam Hours**	**: 03**
	Credits : 03		

Course Objectives:

This course will enable students to:

- Understand characteristics, operation and applications of the diodes, bipolar junction transistors, field effect transistors, SCRs and operational amplifiers in electronic circuits.
- Understand different number systems and working of fundamental building blocks of digital circuits.
- Understand the principle of basic communication system and mobile phones.

MODULE-1

Semiconductor Diodes and Applications:

p-n junction diode, Equivalent circuit of diode, Zener Diode, Zener diode as a voltage regulator, Rectification-Half wave rectifier, Full wave rectifier, Bridge rectifier, Capacitor filter circuit (2.2, 2.3, 2.4 of Text 1).

Photo diode, LED, Photo coupler. (2.7.4, 2.7.5, 2.7.6 of Text 1).

78XX series and 7805 Fixed IC voltage regulator (8.4.4 and 8.4.5 of Text 1).

(RBT Levels : L1, L2 & L3)

MODULE-2

FET and SCR:

Introduction, JFET: Construction and operation, JFET Drain Characteristics and Parameters, JFET Transfer Characteristic, Square law expression for I_D, Input resistance, MOSFET: Depletion and Enhancement type MOSFET-Construction, Operation, Characteristics and Symbols, (refer 7.1, 7.2, 7.4, 7.5 of Text 2), CMOS (4.5 of Text 1).

Silicon Controlled Rectifier (SCR) – Two-transistor model, Switching action, Characteristics, Phase control application (refer 3.4 upto 3.4.5 of Text 1).

(RBT Levels : L1, L2 & L3)

MODULE-3

Operational Amplifiers and Applications:

Introduction to Op-Amp, Op-Amp Input Modes, Op-Amp Parameters-CMRR, Input Offset Voltage and Current, Input Bias Current, Input and Output Impedance, Slew Rate (12.1, 12.2 of Text 2).

Applications of Op-Amp - Inverting amplifier, Non-Inverting amplifier, Summer, Voltage follower, Integrator, Differentiator, Comparator (6.2 of Text 1).

(RBT Levels : L1, L2 & L3)

MODULE-4

BJT Applications, Feedback Amplifiers and Oscillators:

BJT as an amplifier, BJT as a switch, Transistor switch circuit to switch ON/OFF an LED and a lamp in a power circuit using a relay (refer 4.4 and 4.5 of Text 2).
Feedback Amplifiers – Principle, Properties and advantages of Negative Feedback, Types of feedback, Voltage series feedback, Gain stability with feedback (7.1-7.3 of Text 1).
Oscillators – Barkhaunsen's criteria for oscillation, RC Phase Shift oscillator, Wien Bridge oscillator (7.7-7.9 of Text 1).
IC 555 Timer and Astable Oscillator using IC 555 (17.2 and 17.3 of Text 1).

(RBT Levels : L1, L2 & L3)

MODULE-5

Digital Electronics Fundamentals:

Difference between analog and digital signals, Number System-Binary, Hexadecimal, Conversion- Decimal to binary, Hexadecimal to decimal and vice-versa, Boolean algebra, Basic and Universal Gates, Half and Full adder, Multiplexer, Decoder, SR and JK flip-flops, Shift register, 3 bit Ripple Counter (refer 10.1-10.7 of Text 1).
Basic Communication system, Principle of operations of Mobile phone (refer 18.2 and 18.18 of Text 1).

(RBT Levels : L1 & L2)

Course Outcomes:

After studying this course, students will be able to:

- Describe the operation of diodes, BJT, FET and Operational Amplifiers.
- Design and explain the construction of rectifiers, regulators, amplifiers and oscillators.
- Describe general operating principles of SCRs and its application.
- Explain the working and design of Fixed voltage IC regulator using 7805 and Astable oscillator using Timer IC 555.
- Explain the different number system and their conversions and construct simple combinational and sequential logic circuits using Flip-Flops.
- Describe the basic principle of operation of communication system and mobile phones.

Proposed Activities to be carried out for 10 marks of CIE:

Students should construct and make the demo of the following circuits in a group of 3/4 students:

1. +5V power supply unit using Bridge rectifier, Capacitor filter and IC 7805.
2. To switch on/off an LED using a Diode in forward/reverse bias using a battery cell.
3. Transistor switch circuit to operate a relay which switches off/on an LED.
4. IC 741 Integrator circuit/ Comparator circuit.
5. To operate a small loud speaker by generating oscillations using IC 555.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Textbooks:

1. D.P.Kothari, I.J.Nagarath, "Basic Electronics", 2nd edn, Mc Graw Hill, 2018.
2. Thomas L. Floyd, "Electronic Devices", Pearson Education, 9th edition, 2012.

Reference Books:

1. D.P.Kothari, I.J.Nagarath, "Basic Electronics", 1st edn, Mc Graw Hill, 2014.
2. Boylestad, Nashelskey, "Electronic Devices and Circuit Theory", Pearson Education, 9th Edition, 2007/11th edition, 2013.
3. David A. Bell, "Electronic Devices and Circuits", Oxford University Press, 5th Edition, 2008.
4. Muhammad H. Rashid, "Electronics Devices and Circuits", Cengage Learning, 2014.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Course Plan

Course name: Basic Electronics
Course code: 18ELN14/24 AY- 2020-21 (Odd)

Course Contents and Lecture Schedule:

Lesson/ Session No.	Topics	No. of Hours
1.	P-N junction diode, Equivalent circuit of diode	2
2.	Zener Diode, Zener diode as a voltage regulator, Numericals.	2
3.	Rectification-Half wave rectifier, Full wave rectifier, Bridge rectifier, Numericals, Capacitor filter circuit	3
4.	Photodiode,LED, Photocoupler	1
5.	78XX series and 7805 Fixed IC voltage regulator .	1
6.	Difference between analog and digital signals, Number System-Binary, Hexadecimal, Conversion-Decimal to binary, Hexadecimal to decimal and vice-versa,	4
7.	Boolean algebra, Simplification of Boolean expressions, Basic and Universal Gates, Implementation of Boolean functions using logic gates.	2
8.	Logical circuits-Combinational circuits: Half and Full adder, Multiplexer, Decoder	2
9.	SR and JK flip-flops,Sequential circuits: Shift register, 3 bit Ripple Counter(up counting and down counting).	2
10.	Basic Communication system, Principle of operations of Mobile phone	1
11.	Introduction to Op-Amp, Op-Amp Input Modes, Op-Amp Parameters(Ideal and practical)-CMRR. Input Offset Voltage and Current, Input Bias Current, Input and Output Impedance, SlewRate	2
12.	Applications of Op-Amp -Inverting amplifier, Non-Inverting amplifier, Summer, Numericals	2
13.	Voltage follower, Integrator, Differentiator, Comparator , Numericals	2
14.	BJT as an amplifier, BJT as a switch, Numericals. Transistor switch circuit to switch ON/OFF an LED and a lamp in a power circuit using a relay .	2
15.	Feedback Amplifiers -Principle, Properties and advantages of Negative	2

	Feedback, Types of feedback.	
16.	Voltage series feedback, Gain stability with feedback.	1
17.	Oscillators -types of oscillators. Barkhaunsen's criteria for oscillation, RC Phase Shift oscillator, Wien Bridge oscillator, Derivation for frequency of oscillation and condition for sustained oscillations, Numericals.	3
18.	IC 555 Timer: Internal structure and Astable Oscillator using IC 555.	2
19.	Introduction, JFET(n-channel and p-channel): Construction and operation, JFET Drain Characteristics and Parameters, JFET Transfer Characteristic, Square law expression for ID,	4
20.	Parameters, Input resistance, Numericals. MOSFET: Depletion and Enhancement type(n-channel and p-channel)	3
21.	MOSFET-Construction, Operation, MOSFET Characteristics (n-channel and p-channel). Drain characteristics, Transfer characteristics.	1
22.	MOSFET Symbols, Numericals. CMOS Inverter	1
23.	Silicon Controlled Rectifier (SCR) -Two-transistor model, Switching action, Commutation-Forced commutation, Characteristics,	2
24.	Applications of SCR: Phase control application	1
	Total number of Lecture hours	**48**

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Sample T-L Resources

1. https://drive.google.com/file/d/1BdpnkoF7io5rifsFl2poffEmD1dlWig3/view?usp=sharing

2. https://drive.google.com/drive/u/1/folders/1kN_CDX6StG6lL2ovuvqv_OhBHhh6Srav

BMS INSTITUTE OF TECHNOLOGY & MANAGEMENT,

YELAHANKA, BANGALORE-64

Batch: 2020 - 21 **Branch: ECE**

SL. NO.	USN	NAME OF THE CANDIDATE
1.	1BY20EC001	AAKASH KUMAR SINGH
2.	1BY20EC002	AASHRITHA M
3.	1BY20EC003	ABHAY SINGH
4.	1BY20EC004	ABHISHEK K
5.	1BY20EC005	ABHISHEK KUMAR
6.	1BY20EC006	ABHISHEK NAGESH SHETTY
7.	1BY20EC007	ABHISHEK YADAV
8.	1BY20EC008	ACHYUTH RAO H
9.	1BY20EC009	ACHYUTHA GOWDA C P
10.	1BY20EC010	ADIKE TEJA
11.	1BY20EC011	ADITHYA R

12.	1BY20EC012	ADITYA SRINIVAS K
13.	1BY20EC013	AISHWARYA N
14.	1BY20EC014	AJAY BASHA KOMALI
15.	1BY20EC015	AKHIL M P
16.	1BY20EC016	AKHILESH N
17.	1BY20EC017	AKSHATA SUBHASH DABRABAD
18.	1BY20EC018	AKSHATHA S
19.	1BY20EC019	AKSHAY A GOUDAR
20.	1BY20EC020	AKSHAYA SUBRAHMANYA E
21.	1BY20EC021	ALLA VAMSI KRISHNA
22.	1BY20EC022	AMAN KUMAR
23.	1BY20EC023	AMOGH C DIXIT
24.	1BY20EC024	AMULYA M KAUSHIK
25.	1BY20EC025	ANAND A B
26.	1BY20EC026	ANANYA R
27.	1BY20EC027	ANIKET SHARMA
28.	1BY20EC028	ANNAM SASI SEKHAR

29.	1BY20EC029	ANUBHAV KUMAR
30.	1BY20EC030	APOORV SHANDILYA
31.	1BY20EC031	ARCHANA B
32.	1BY20EC032	ARUNABH RANJAN
33	1BY20EC033	ARYA MURALI
33.	1BY20EC034	ASHISH SRINIVASAN
34.	1BY20EC035	ASWIN AJAY A
35.	1BY20EC036	ASIF AYOUB BHATTI
36.	1BY20EC037	ATISH MARAGUR
37.	1BY20EC038	B MEGHANA
38.	1BY20EC039	BHASWATI TALUKDAR
39.	1BY20EC040	BHAVITHA D S
40.	1BY20EC041	BHEEMI REDDY HARINI
41.	1BY20EC042	BHUMIKA R
42.	1BY20EC043	BHUMIKA T V
43.	1BY20EC044	BHUVAN A R
44.	1BY20EC045	BHUVANA H

45.	1BY20EC046	BITTU KUMAR
46.	1BY20EC047	CHANDANA A
47.	1BY20EC048	CHANDINI KUMARI
48.	1BY20EC049	CHANDU B R
49.	1BY20EC050	CHARAN G S
50.	1BY20EC051	CHIRAG KUMAR N
51.	1BY20EC052	DEEKSHITHA B S
52.	1BY20EC053	DEEPAK DARSHAN P
53.	1BY20EC054	DEEPIKA R
54.	1BY20EC055	DEEPTI H P
55.	1BY20EC056	DEVARAJ
56.	1BY20EC057	DHARANI S
57.	1BY20EC058	DIVYASHREE S
58.	1BY20EC059	DUGGASANI VENKATA PRADEEP KUMAR REDDY
59.	1BY20EC060	ENOSH J
60.	1BY20EC061	G MEENAKSHI

61.	1BY20EC062	G THARUN
62.	1BY20EC063	GAGANDEEP S
63.	1BY20EC064	GANDLAPARTHI NAVYATHA
64.	1BY20EC065	GANGARAJU KUSHAL VARMA
65.	1BY20EC066	GAURAV R N
66.	1BY20EC067	GAYATHRI MENON
67.	1BY20EC068	GONIGUNTLA VARSHITH
68.	1BY20EC069	H C SIDDHARTHA REDDY
69.	1BY20EC070	IRENE MARIA DANIEL
70.	1BY20EC071	ISHIKA KUMARI
71.	1BY20EC072	ISHITA CHOUDHARY
72.	1BY20EC073	JAHNAVI K N
73.	1BY20EC074	JAYANTH J
74.	1BY20EC075	JEEVAN V
75.	1BY20EC076	K SAI KISHAN
76.	1BY20EC077	K V DIVYANSH
77.	1BY20EC078	KAMALESH JENA

78.	1BY20EC079	KARTHIK R
79.	1BY20EC080	KATARU YOHITHA
80.	1BY20EC081	KAUSHALENDRA SINGH
81.	1BY20EC082	BELLARY KEERTHI
82.	1BY20EC083	KUDUMALA SHANMUKHA VENKATA SUMANTH REDDY
83.	1BY20EC084	KUMUDA V
84.	1BY20EC085	KUNJETI MANIDEEP
85.	1BY20EC086	KUSHAGRA
86.	1BY20EC087	LALITH P
87.	1BY20EC088	LATHA N
88.	1BY20EC089	LEELA M N
89.	1BY20EC090	LETI MANISH KUMAR
90.	1BY20EC091	LITESH KUMAR M
91.	1BY20EC092	LLOYD SWEEBERT LEWIS
92.	1BY20EC093	MADEM NITHIN DATTA REDDY
93.	1BY20EC094	MANAS SINGH

94.	1BY20EC095	MARISETTY SAI PRAGNA
95.	1BY20EC096	MD AHKAM TANVEER
96.	1BY20EC097	MD FARHAN
97.	1BY20EC098	MEGHANATHA REDDY P
98.	1BY20EC099	MENAKARU SRIKANTH REDDY
99.	1BY20EC100	MISBA AZEEZA
100.	1BY20EC101	MOHAMMED SAQIB
101.	1BY20EC102	MOHAMMED YUNUS
102.	1BY20EC103	MOHD YASIR
103.	1BY20EC104	MULA MAHESWAR REDDY
104.	1BY20EC105	N SOUNDARYA
105.	1BY20EC106	N Y SHREYAS
106.	1BY20EC107	NEKKALAPUDI GREESHMA CHOWDARY
107.	1BY20EC108	NEVAN GEORGE THOMAS
108.	1BY20EC109	NIKHIL S
109.	1BY20EC110	NISARGA M
110.	1BY20EC111	NISHANT KUMAR

111.	1BY20EC112	NISHMITHA ANTON RODRIGUES
112.	1BY20EC113	O SHANKAR NAIDU
113.	1BY20EC114	P PRAVEEN KUMAR
114.	1BY20EC115	P S AAKASH
115.	1BY20EC116	PALAVALI HASWANTH REDDY
116.	1BY20EC117	PARUCHURI SREENIJA
117.	1BY20EC118	PONNAM NAGA SRAVAN REDDY
118.	1BY20EC119	POTTIPATI SAIKIRAN REDDY
119.	1BY20EC120	PRABHULING
120.	1BY20EC121	PRANAV B C
121.	1BY20EC122	PRANAV SHAKTHI S
122.	1BY20EC123	PRASHANTH G
123.	1BY20EC124	PRATHIK S
124.	1BY20EC125	PRAVIN M MALASHETTI
125.	1BY20EC126	PREETHI R POOJARY
126.	1BY20EC127	R SHREEYA REDDY
127.	1BY20EC128	RAHUL KUMAR

128.	1BY20EC129	RAHUL KUMAR
129.	1BY20EC130	RAHUL SHINDHE
130.	1BY20EC131	RAHUL VENK K
131.	1BY20EC132	RAKSHA B R
132.	1BY20EC133	RAKSHIT GOVIND T
133.	1BY20EC134	RAKSHITH G M
134.	1BY20EC135	RAKSHITH S
135.	1BY20EC136	RISHABH JAISWAL
136.	1BY20EC137	RITIK RANJAN SINGH
137.	1BY20EC138	ROHIT PRASAD MAHINDRAKAR
138.	1BY20EC139	S KEDHAR SIMHA
139.	1BY20EC140	S M VARASIDHI VINAYAKA
140.	1BY20EC141	PRASHANTH S
141.	1BY20EC142	SAHANA N
142.	1BY20EC143	SAHANA V
143.	1BY20EC144	SAHIL SHARAN
144.	1BY20EC145	SAMBHAIAHPALEM SURENDRA

145.	1BY20EC146	SANDEEP TORAN
146.	1BY20EC147	SANJANA D R
147.	1BY20EC148	SANSKRITI
148.	1BY20EC149	SHAMANTH H
149.	1BY20EC150	SHARAN S
150.	1BY20EC151	SHASHANK M E
151.	1BY20EC152	SHIKHAR PAL
152.	1BY20EC153	SHIVA KUMAR P
153.	1BY20EC154	SHRAVANI B K
154.	1BY20EC155	SHREEVALYA S N
155.	1BY20EC156	SHREYA G D
156.	1BY20EC157	SHREYASHI SINGH
157.	1BY20EC158	SHRISTI BAISHYA
158.	1BY20EC159	SHRIVANTH RAJ N
159.	1BY20EC160	SHUBHAM
160.	1BY20EC161	SHUBHAM KUMAR SINGH
161.	1BY20EC162	SIDDARTH CHANDEL

162.	1BY20EC163	SIMRAN GUPTA
163.	1BY20EC164	SINCHANA NAG G S
164.	1BY20EC165	SPOORTHI M
165.	1BY20EC166	SRIDHAR S
166.	1BY20EC167	SRUSHTI R
167.	1BY20EC168	SUCHETHA P B
168.	1BY20EC169	SUDEEP V
169.	1BY20EC170	SUHAS S
170.	1BY20EC171	SURYA PRAKASH H N
171.	1BY20EC172	SWATHI A M
172.	1BY20EC173	SWATHI G S
173.	1BY20EC174	TANNU KUMARI
174.	1BY20EC175	TEJASWINI R
175.	1BY20EC176	TERENCE PRABHU BARRAT
176.	1BY20EC177	THEJASWINI H A
177.	1BY20EC178	TUSHAR JAIN
178.	1BY20EC179	TUSHAR N

179.	1BY20EC180	VAISHNAVI
180.	1BY20EC181	VANCHIREDDY DEEPIKA
181.	1BY20EC182	VARSHA V
182.	1BY20EC183	VARUN S
183.	1BY20EC184	VIKAS REDDY H V
184.	1BY20EC185	VIKASH KUMAR
185.	1BY20EC186	VINAYAKA REDDY B KONDIKOPPA
186.	1BY20EC187	VISHAL RAJ
187.	1BY20EC188	VISHVA RAJ R
188.	1BY20EC190	YASH KUMAR
189.	1BY20EC191	YASHODHA S SHRIDHAR
190.	1BY20EC192	YASHWANTH T
191.	1BY20EC193	YASMEEN TAJ H

BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT
Avalahalli, Doddaballapur Main Road, Bengaluru - 560064

FIRST INTERNAL ASSESSMENT, JANUARY 2020-2021

Name of the Course: Basic Electronics	Course Code: 18ELN14	Branch &Semester: ECE I SEM(H,I,J section)
Max. Marks : 50	Date: 29 .01.2021	Time: 2.00-3.30P.M
Course Coordinators: Dr. Surekha .R.Gondkar, Dr.Vijayalakshmi,Chandra prabha.R		

Note: *Answer* ***THREE*** *full questions from* ***Part A*** *and* ***Part B*** *questions are compulsory. Assume any missing data.*

Qn. No.	PART A	Marks	CO
1.	Simplify and realize the following Boolean expressions using Universal gates (i)Y= $(A+\overline{B}+\overline{C})(A+\overline{B}+C)$ ((ii) R=$(XYZ+YZ+\overline{Z})$	5+5	CO3,K3
	OR		
2.	Perform the binary subtraction using (a) 1's Compliment (b) 2's Compliment (i) $(67)_{10}$-$(89)_{10}$ (ii)$(489)_{10}$-$(343)_{10}$	5+5	CO3,K2
3.	a)Simplify and realize the following Boolean expressions using logic gates (i) Y= C(B+C)(A+B+C) (ii)Y= $\overline{\overline{BC}+\overline{AD}(\overline{AB}+\overline{CD})}$ b) state and prove De-Morgans theorem for the three input variables	5+5	CO3,K3
	OR		
4.	a)Simplify $S = A \oplus B \oplus C$ and realize using basic gates. b)Convert (i) $(110111.11101)_2$ = ( )$_{16}$, (ii)$(ADEF.09)_{16}$ = ( )$_{10}$, (iii)$(0957.945)_{10}$=( )$_{16}$	4+6	CO3 K3
5.	Design a circuit which selects one output from a group of 8 inputs.	10	CO3,K3
	OR		
6.	Design a combinational Full adder circuit using two half adders.	10	CO3,K3
	PART B		
7.	Digital circuits have many applications in real times. One such application is water pump operation. Pump will operate if there is insufficient amount of water in the tank inside the house and sufficient amount of water in the well. If there is sufficiency of water in the tank inside the house and insufficiency of water in the well, yellow indicator light will light up. If there is insufficiency of water both in the tank inside the house and in the well, red indicator light will light up and it should be alarmed to the owner only in the case of red light. Implement the given real time task using digital circuits (logic gates/derived gates).	10	CO4, K4
8	From the case study material, Design the parity generator which generates even and odd parity.	10	CO4,PO2, K3

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Avalahalli, Doddaballapur Main Road, Bengaluru - 560064

FIRST INTERNAL ASSESSMENT, JANUARY 2020-2021

CO1	Understand the operation of semiconductor devices and circuits.
CO2	Apply the knowledge of basics of semiconductor devices to build electronic circuits.
CO3	Analyze the working of analog and digital circuits for any application.
CO4	Design electronic systems using analog and digital devices.
CO5	Design and demonstrate(Hardware/simulation) the basic applications of electronic circuits

Remembering (K1)	**Understanding (K2)**	**Applying (K3)**	**Analyzing (K4)**	**Evaluating (K5)**	**Creating (K6)**

Course Coordinator(s)	Module Coordinator(s)	Program Coordinator	Head of the Department 27/11/2021

**********GOOD LUCK**********

BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

Avalahalli, Doddaballapur Main Road, Bengaluru - 560064

SECOND INTERNAL ASSESSMENT TEST, FEBRUARY- 21

Course Name	Basic Electronics	**Course Code**	18ELN14
Branch & Semester	I ECE H, I and J	**Date**	26/02/2021
Name of the Course Coordinator (s)	Dr. Surekha R Gondkar Mrs. Chandraprabha R Dr. Vijayalakshmi G V	**Max. Marks**	50
		Time	11:00-12:15PM

Note: Answer FIVE full questions:
1. Answer 3 full questions from Part-A.
2. Part – B is compulsory.

Q. No	PART A	Marks	CO
1.	a) Explain the following terms related to op-amp (i) CMRR (ii) Input offest Voltage and Current (iii) Slew rate and (iv) PSRR b) Design an adder circuit using an op-amp to obtain an output voltage of Vo = - [2V1+3V2+5V3]	4+6M	CO3 K3
	OR		
2.	a) With a neat diagram, explain how an op-amp can be used as a differentiator. b) A non-inverting amplifier circuit has an input resistance of 10KΩ and feedback resistance 60KΩ with load resistance of 47KΩ. Draw the circuit. Calculate the output voltage, voltage gain, load current when the input voltage is 1.5V.	4+6M	CO3 K3
3.	a) Derive the equation for frequency of oscillation and gain of Wien bridge oscillator. b) The frequency sensitivity arms of the Wein bridge oscillator uses $C_1 = C_2 = 0.01$ μF and $R_1 = 10$ kΩ while R_2 is kept variable. The frequency is to be varied from 10 kHz to 50 kHz by varying R_2. Find the minimum and maximum values of R_2.	6+4M	CO3 K3
	OR		
4.	a)Define an oscillator. Explain the Barkhausens' criteria for oscillations. b)Explain the operation of an RC phase shift oscillator with circuit diagram and necessary equations.	4+6 M	CO3 K2
5.	a) Explain the working of a clocked SR flip-flop with the help of a logic diagram and truth table. b) Design a asynchronous counter which counts from 0 to 7.	10M	CO4 K3
	OR		
6.	a)What is a shift register? Design a 4-bit SISO shift register to shift the data [1011] and also show its working using truth table. b) Explain the elements of communication system with a neat block diagram.	10 M	CO4 K3
	PART B		
7.	A Register is a device which is used to store information. The information stored within these registers can be transferred with the help of shift registers. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses. Design a clock generator using multivibrator to carry out the above task.	10 M	CO4 K4
8.	The mobile technology has presently transformed the world and has made life and business much easier. With reference to the case study material, explain GSM architecture with a neat block diagram, highlighting all the interfaces.	10 M	CO3 K2

BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

Avalahalli, Doddaballapur Main Road, Bengaluru - 560064

SECOND INTERNAL ASSESSMENT TEST, FEBRUARY- 21

Course Outcomes (COs)

CO1	Understand the operation of semiconductor devices and circuits.
CO2	Apply the knowledge of basics of semiconductor devices to build electronic circuits.
CO3	Analyse the working of analog and digital circuits for any application.
CO4	Design electronic systems using analog and digital devices.
CO5	Design and demonstrate(Hardware/simulation) the basic applications of electronic circuits.
Blooms Levels	Remember(K1) Understand(K2) Apply(K3) Analyze(K4) Evaluate(K5)

Signatures of the Question Paper Scrutiny Committee

			23/2/21
Course Coordinator(s)	**Module Coordinator(s)**	**Program Coordinator**	**Head of the Department**

BMS INSTITUTE OF TECHNOLOGY & MANAGEMENT

YELAHANKA – BANGALORE - 64

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

THIRD INTERNAL EXAMINATION, SEPTEMBER-2021

Subject: BASIC ELECTRONICS	*Subject Code: 18ELN24*	*Branch & Semester : ISE II-D,E&F SECTIONS*
Max. Marks : 50	*Date: 21-09-2021* *Time:2.00 to 3.30PM*	*Course Coordinators:* *Dr.SRG,CP,SB*

Note: Answer THREE full questions from PART A, and Part B questions are compulsory.

Qn. No.	PART A	Marks	CO
1	Explain the working of a PN junction diode under forward and reverse biasing with neat diagrams and graphs.	*10M*	CO1,K2
	OR		
2	Explain the working of an LED, Photodiode and a Photocoupler with neat diagrams.	*10M*	CO1,K2
3	With neat circuit diagram and waveforms, explain the working of a full wave bridge rectifier. Show that its efficiency is 81%.	*10M*	CO2,K3
	OR		
4	What is negative feedback? List the advantages of negative feedback. Explain the voltage series feedback amplifier and derive an expression for voltage gain	*10M*	CO2,K3
5	Explain the operation of half wave rectifier with capacitor filter with neat circuit diagram and waveforms	*10M*	CO1,K2
	OR		
6	List the differences between BJT and FET. Explain the drain and transfer characteristics of a n-channel JFET with neat circuit diagram and graphs.	*10M*	CO1,K2
	PART B		
7	Analyze the characteristics of a Zener diode to use it for regulation purpose. Demonstrate with a neat circuit diagram how it can be used as a voltage regulator.	*10M*	CO3, K4
8	With reference to the case study on "Applications of transistor as a switch" illustrate with neat circuit diagrams, how transistor can be used as a ON/OFF switch and any one of its application.	*10M*	CO3, K3

***Course outcomes:** Students will be able to -*

1.	*Understand the operation of semiconductor devices and circuits.*
2.	*Apply the knowledge of basics of semiconductor devices to build electronic circuits.*
3.	*Analyze the working of analog and digital circuits for any application.*
4.	*Design electronic systems using analog and digital devices.*
5.	*Design and demonstrate(Hardware/simulation) the basic applications of electronic circuits*

BLOOM'S LEVEL

K1: Remember K2:Understand K3: Apply K4: Analyze K5: Evaluate K6: Creation

Signatures of the question paper Scrutiny Committee

Sg. 18/9/21	18/9/21		
Course coordinators	**Module Coordinator(s)**	**Program Coordinator**	**Head of the Department**

BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT
Avalahalli, Doddaballapur Main Road, Bengaluru - 560064

Course Name	Basic Electronics	**Course Code**	18ELN14
Branch & Semester	I ECE H, I and J	**Date**	01/04/2021

Basic electronics

Assignment:5_ marks
To be submitted in proper format
Date of submission: 08/04/2021

1) List the ideal features of Op-amp.
2) Draw and explain the operation of two transistor model of SCR.
3) Explain the CMOS as inverter.
4) Explain the characteristic of n channel JFET.
5) Derive the expression for voltage gain for an inverting opamp.
6) Explain the working model of n channel JFET.
7) Explain the working of opamp Comparator.
8) Draw and Explain the VI Characteristics OF SCR
9) Derive the output voltage for opamp as an integrator differentiator and subtractor, non-inverting amplifier, inverting summer
10) Explain the working model and characteristics of n channel enhancement MOSFET
11) Explain the working model and characteristics of n channel depletion MOSFET
12) Explain the operation of SCR as phase controlled Rectifier
13) Write a note on forced commutation/turnoff.
14) Problems to find drain current(formulas)

Course Outcomes (COs)

CO1	Understand the operation of semiconductor devices and circuits.
CO2	Apply the knowledge of basics of semiconductor devices to build electronic circuits.
CO3	Analyse the working of analog and digital circuits for any application.
CO4	Design electronic systems using analog and digital devices.
CO5	Design and demonstrate(Hardware/simulation) the basic applications of electronic circuits.

BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

YELAHANKA – BANGALORE - 64

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Activity

Dear students , Prepare a poster on the assigned topic in a team and submit the report

REPORT CONTENT: Explanation, circuit,real time application and results

SL	NAME	TOPIC
1	ARYA MURALI	Transistor as in inverter
2	CHIRAG KUMAR N	
3	N SOUNDARYA	
4	NISARGA M	
5	PRASHANTH G	Simulation of all logic gates
6	PREETHI R POOJARY	
7	RAKSHITH S	
8	SHARAN S	
9	VIKAS REDDY H V	Application of opamps _integrator
10	MISBA AZEEZA	
11	PRATHIK S	
12	SUDEEP V	
13	PRAVIN M MALASHETTI	Application of opamps _adder
14	B MEGHANA	
15	BHUMIKA T V	
16	LEELA M N	
17	CHANDU B R	Application of opamps _differentiator
18	VIVEK KUMAR	
19	MULA MAHESWAR REDDY	
20	GAURAV R N	
21	PALAVALI HASWANTH REDDY	Application of opamps _non inverting amplifier
22	AJAY BASHA KOMALI	
23	SIDDARTH CHANDEL	
24	MENAKARU SRIKANTH REDDY	
25	AMULYA M KAUSHIK	Application of opamps _inverting amplifier
26	LALITH P	
27	DEEPIKA R	
28	G MEENAKSHI	
29	SRIDHAR S	Application of opamps _subtractor
30	DHARANI S	
31	ANAND A B	

32	SHREEVALYA S N	
33	SHASHANK M E	Application of opamps _voltage follower
34	SHRAVANI B K	
35	ATISH MARAGUR	
36	SANDEEP TORAN	
37	RAKSHA B R	Weinsbrigeocillators
38	TUSHAR N	
40	O SHANKAR NAIDU	
41	SHAMANTH H	
42	ANANYA R	RC Phase shift Oscillator
43	SWATHI A M	
44	KARTHIK R	
45	KUNJETI MANIDEEP	
46	SHREYASHI SINGH	Mux
47	MARISETTY SAI PRAGNA	
48	VAISHNAVI	
49	N Y SHREYAS	
50	GANGARAJU KUSHAL VARMA	Decoder
51	ROHIT PRASAD MAHINDRAKAR	
52	KUSHAGRA	
53	ADIKE TEJA	
54	TUSHAR JAIN	Full wave rectifier
55	RAHUL KUMAR	
56	KAMALESH JENA	
57	AKSHAY A GOUDAR	
58	ABHISHEK KUMAR	Half wave rectifier
59	AMAN KUMAR	
60	POTTIPATI SAIKIRAN REDDY	
61	SAMBHAIAHPALEM SURENDRA	
62	DUGGASANIVENKATA PRADEEP KUMAR REDDY	

B.M.S. Institute of Technology And Management

Affiliated to the Visvesvaraya Technological University, Belgaum.

POSTER TOPIC: SIMULATION OF LOGIC GATES

Introduction

A logic gate is an idealized model of computation or physical electronic device implementing a Boolean function, a logical operation performed on one or more binary inputs that produces a single binary output.

TYPES:

1. Basic Gates- AND, OR, NOT.
2. Universal Gates- NAND ,NOR.
3. Derived Gates- XOR,XNOR.

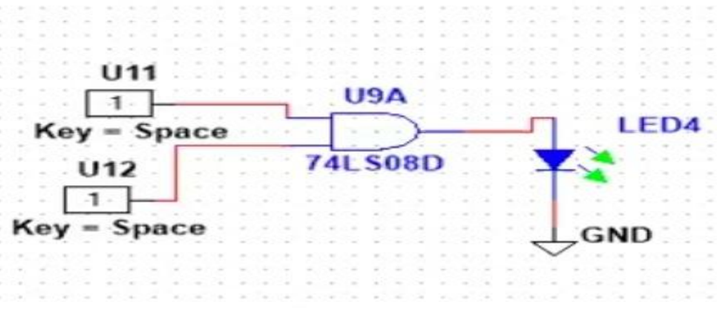
Working principle with neat figures

BASIC GATES

AND GATE:

INPUT :A,B
OUTPUT:Y=A.B

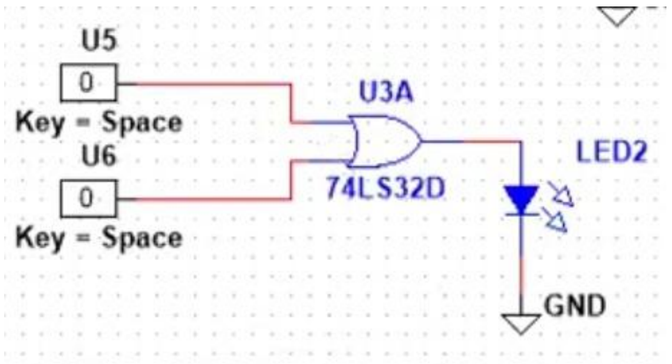
Input		Output
A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1



OR GATE:

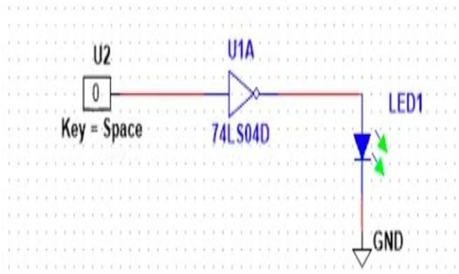
INPUT: A,B
OUTPUT: Y=A+B

Input		Output
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1



NOT GATE:

INPUT : A
OUTPUT : INVERSE OF A



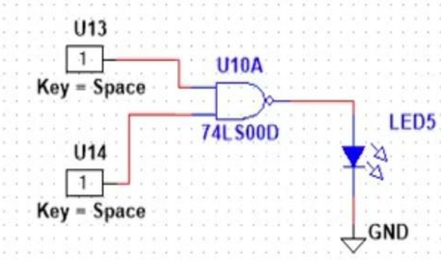
Input A	Output X=$\overline{A}$
0	1
1	0

Output is inverse of Input

UNIVERSAL GATES:

NAND GATE:

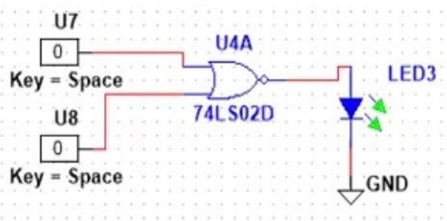
INPUT:A,B
OUTPUT :Y =INVERSE OF A.B



Input		Output
A	B	Y= $\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

NOR GATE:

INPUT:A,B
OUTPUT:Y=INVERSE OF A+B



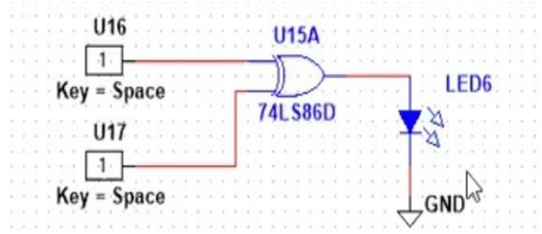
Input		Output
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

DERIVED GATES:

XOR (EXCLUSIVE OR):

$$A \cdot \overline{B} + \overline{A} \cdot B$$
$$A + B) \cdot (\overline{A} + \overline{B})$$

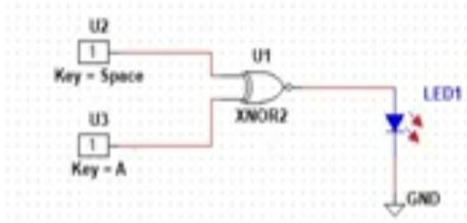
$C = A \oplus B$ (Input1, Input2, Output)



INPUT		OUTPUT
A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

XNOR GATE:

Output $C = A \odot B$ Input 1, Input 2



Input		Output
A	B	A XNOR B
0	0	1
0	1	0
1	0	0
1	1	1

Advantages

1. Logic Gates are quick yet use low energy .
2. Logic Gates don't get overworked.
3. Logic Gates can lessen the prescribed number of I/O ports needed by a microcontroller.
4. Logic Gates can bring about straightforward data encryption and decryption.

Disadvantages :

1. Operating voltage is limited.
2. Time delay occurs between input and output.

Applications

1. The applications of Logic Gates are: NAND Gates are used in Burglar alarms and buzzers.
2. They are basically used in circuits involving computation and processing. They are also used in push button switches.
3. The important applications of Logic Gates in Digital Electronics are Flip-Flop circuit, register, digital counter, Microprocessor, Microcontroller, etc.

DONE BY:

SHARAN S
PREETHI R
RAKSHITH
PRASHANTH G

18ELN14/24

Visvesvaraya Technological University, Belagavi

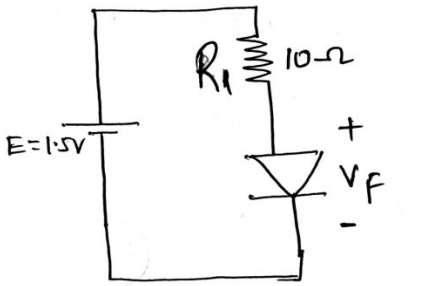
MODEL QUESTION PAPER

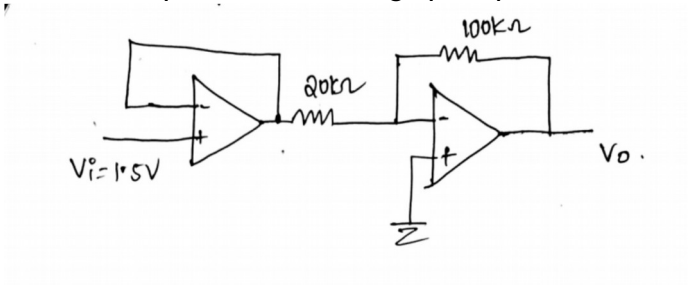
1st/2nd Semester, B.E (CBCS 2018-19 Scheme)

Course: 18ELN14/24- BASIC ELECTRONICS – *Set no.1*

Time: 3 Hours **Max. Marks: 100**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	Marks
1	a	Explain the operation of p-n junction diode under forward and reverse biased condition	8
	b	Explain how Zener diode can be used as a voltage regulator	6
	c	A diode circuit shown below has E=1.5V, R_1=10 ohm. By assuming V_f=0.7V, calculate I_f for i) $r_d = 0$ ii) r_d = 0.25 ohm  Fig.Q.1(c)	6
		OR	
2	a	With a neat circuit diagram and waveform, explain the working of half-wave rectifier and derive the expression for average load current.	8
	b	Explain briefly the operation of a capacitor filter circuit.	6
	c	Explain the operation of 7805 fixed IC voltage regulator.	6
		Module-2	

3	a	Explain the characteristics of N-channel JFET.	8
	b	For E-MOSFET, determine value of I_D, if I_D (ON)= 4mA, V_{gs}(ON)=6V, V_T=4V and V_{gs}=8V.	4
	c	Explain the construction and working of P-channel enhancement type MOSFET.	8
		OR	
4	a	Draw and explain the operations of SCR using 2-transistor equivalent circuit.	8
	b	Explain phase controlled application of SCR.	6
	c	Explain the operation of a CMOS inverter.	6
		Module-3	
5	a	For an op-amp (i) List the characteristics of an ideal op-amp and (ii) Draw the three input inverting summer circuit and derive an expression for its output voltage.	8
	b	Define the terms i) Slew rate ii) CMRR iii) Common mode gain A_C of op-amp	6
	c	Design an adder circuit using an op-amp to obtain an output voltage of V_o= -[$2V_1$+$3V_2$+$5V_3$]	6
		OR	
6	a	Draw the working of an inverting op-amp. Derive the expression for its voltage gain.	8
	b	With a neat diagram, explain how an op-amp can be used as a differentiator.	6
	c	Find the output V_o of following op-amp circuit.  Fig.Q.6(c)	6

		Module-4	
7	a	Explain the operation of BJT as an amplifier and as a switch.	8
	b	What is a feedback amplifier? Briefly explain different types of feedback amplifiers.	6
	c	Draw and explain the operation of a voltage series feedback amplifier and derive an expression for its voltage gain with feedback.	6
		OR	
8	a	Explain the Barkhausens' criteria for oscillations.	6
	b	Explain the operation of an RC phase shift oscillator.	6
	c	Explain the working of an Astable oscillator constructed using IC- 555 timer.	8
		Module-5	
9	a	Convert the following. i) $(725.25)_{10}=(\ ?\ )_2 = (\ ?\ )_{16}$ ii) $(111100111110001)_2= (\ ?\ )_{10} = (\ ?\ )_{16}$	8
	b	Simplify the following expressions and draw the logic circuits using basic gates. i) AB+$\acute{A}C+A\acute{B}C$ (AB+C) ii) (A+$\acute{B}$)(CD+E)	6
	c	Realize a full adder circuit using 2 half adders.	6
		OR	
10	a	What is a multiplexer? Explain the working of 4:1 multiplexer.	6
	b	With the help of a logic diagram and truth table, explain the working of a clocked SR flip-flop.	6
	c	What is a shift register? Explain the working of a 4-bit SISO shift register.	8

****

18ELN14/24

Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER

1st/2nd Semester, B.E (CBCS 2018-19 Scheme)

Course: 18ELN14/24- BASIC ELECTRONICS – *Set no. 2*

Time: 3 Hours **Max. Marks: 100**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

		Module-1	Marks
1	a.	Explain the operation of PN junction diode under forward and reverse bias conditions	6M
	b.	A full wave bridge rectifier with an input of 100V(rms) feeds a load of 1kΩ .V_T=0.7V (i) If the diodes employed are of silicon, what is the dc voltage across the load? (ii) Determine the PIV rating of each diode.. (iii) Determine the maximum current that each diode conducts and the diode power rating.	6M
	c.	Write a short note on (i) Light emitting diode and (ii) Photo coupler	8M
		OR	
2	a.	What is Zener diode? With neat circuit diagram, explain the operation of a voltage regulator with and without load?	8M
	b.	A silicon diode has I_S=10nA operating at 25°C. Calculate I_n for a forward bias of 0.6V.	4M
	c.	Define rectifier. Sketch a centre tapped full wave rectifier and derive the following. Show the appropriate waveforms. (i) Average Voltage (ii) Efficiency and (iii) Ripple factor	8M
		Module-2	
3	a.	Explain the construction and operation of JFET with necessary diagram.	7M
	b.	Draw and explain the V-I characteristics of SCR.	6M
	c.	With neat circuit diagram, explain the working of CMOS inverter.	7M
		OR	
4	a.	What is MOSFET? Explain D- MOSFET and E- MOSFET transfer characteristics.	8M
	b.	A certain JFET has an I_{GSS} of -2nA for V_{GS}= -20V Determine the input resistance.	4M
	c.	What is SCR? Explain the working of two transistor model of SCR.	6M
		Module-3	
5	a.	Describe the characteristics of basic Op-Amp. List out its ideal characteristics.	8M
	b.	A certain op-amp has an open loop voltage gain of 1,00,000 and a common mode gain of 0.2. Determine the CMRR and express it in decibels.	4M
	c.	Derive the output voltage for the following (i) Integrator and (ii) Voltage follower	8M

		OR	
6	a.	Explain the following terms related to op-amp (i) CMRR (ii) Offest Voltage and Current (iii) Slew rate and (iv) Input bias	8M
	b.	Design an adder using op-amp to give the output voltage $V_O = -[2V_1+3V_2+5V_3]$.	6M
	c.	Derive the output voltage of a non-inverting amplifier.	6M
		Module-4	
7	a.	What is an amplifier? Explain the operation of transistor amplifier circuit.	8M
	b.	Define feedback amplifier? With necessary diagram and equation explain the different types of feedback?	12M
		OR	
8	a.	Briefly explain how a transistor is used as an electronic switch.	6M
	b.	Explain how 555 timer can be used as an oscillator.	6M
	c.	Define an oscillator? Derive the equation for Wien bridge oscillator.	8M
		Module-5	
9	a.	Perform the following (i) Convert $(A\ B\ C\ D)_{16}=(?)_2=(?)_8=(?)_{10}$ (ii) Subtract $(1010)_2-(111)_2$ using 2's compliment method.	5M
	b.	Realize Y=AB+CD+E using NAND gates.	4M
	c.	What is a flip flop? Explain the Master Slave JK flip flop operation.	5M
	d.	With a neat block diagram explain GSM system.	6M
		OR	
10	a.	Perform the following (i) Convert $(111110101101)_2$ to $(\ )_8$ (ii) Subtract $(22)_2-(17)_2$ using 1's and 2's compliment method.	5M
	b.	Design full adder circuit using three variables and implement it using two half adders.	8M
	c.	What is a counter? With a neat timing and block diagram, explain three bit asynchronous counter operation.	7M

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18ELN14/24

Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER

1st / 2nd Semester, B.E (CBCS)

Course: 18ELN14/24- Basic Electronics – *Set no. 3*

Note: (i) Answer five full questions selecting any one full question from each module.
(ii) Missing data may be suitably assumed

Time: 3 Hrs **Max. Marks: 100**

MODULE 1			
1	a	Explain the forward and reverse bias condition for a pn junction diode with neat diagram.	08M
	b	A half wave rectifier is fed from a supply of 230 V, 50 Hz with step down transformer of ratio 3:1. Resistive load connected is 10 KΩ. The diode forward resistance is 75Ω and transformer secondary is 10 Ω. Calculate the DC load current, DC load voltage, efficiency and ripple factor.	06M
	c	Write a short note on the following: (i) Photo diode (ii) Light emitting diode	06M
OR			
2	a	With neat circuit diagram and wave forms explain the working of a centre tapped full wave rectifier.	08M
	b	A Zener diode has a breakdown voltage of 10V. It is supplied from a voltage source varying between 20-40V in series with a resistance of 820Ω. Using an ideal Zener model, obtain the minimum and maximum Zener currents	06M
	c	Explain the features of LM7805 fixed regulator.	06M
MODULE 2			
3	a	Explain the construction and operation of a p-channel JFET	08M
	b	With neat diagram explain the operation of a CMOS inverter.	06M
	c	With neat diagram explain the VI characteristics of an SCR.	06M
OR			
4	a	Explain the characteristics of an n-channel JEFT.	06M
	b	With neat diagram, explain the characteristics of a enhancement type MOSFET.	08M
	c	With neat diagram explain the two transistor model of an SCR.	06M

MODULE 3			
5	a	Explain the following with respect to op-amp (i) Input Impedance (ii) output impedance (iii) Slew rate (iv) CMRR (v) virtual ground	10M
	b	Derive an expression for the output voltage of an inverting amplifier.	06M
	c	The input to the basic differentiator circuit is a sinusoidal voltage of peak value of 10mV and frequency 1.5KHz. Find the output if, Rf=100KΩ and C1=1μF.	04M
OR			
6	a	Derive an expression for the output voltage of an op-amp integrator.	06M
	b	Derive an expression for the output voltage of an inverting summer.	06M
	c	A non-inverting amplifier circuit has an input resistance of 10KΩ and feedback resistance 60KΩ with load resistance of 47KΩ. Draw the circuit. Calculate the output voltage, voltage gain, load current when the input voltage is 1.5V.	08M
MODULE 4			
7	a	Explain how the transistor can be used as a switch and as an amplifier.	10M
	b	An amplifier has a high frequency response described by $A=\frac{A0}{1+(j\omega/\omega 2)}$. Where in A_0=1000, ω_2=104 rad/s. Find the feedback factor which will raise the upper corner frequency ω_2 to 105 Hz. What is the corresponding gain of the amplifier? Find also the gain bandwidth product in this case.	04M
	c	With a neat circuit diagram, explain the working of RC phase shift oscillator.	06M
OR			
8	a	List the advantages of negative feedback in an amplifier. Explain the voltage series feedback amplifier. Show that the gain band width product for a feedback amplifier is constant.	10M
	b	The frequency sensitivity arms of the Wein bridge oscillator uses C_1=C_2=0.01μF and R_1=10KΩ while R_2 is kept variable. The frequency is to be varied from 10KHz to 50 KHz by varying R_2. Find the minimum and maximum values of R_2.	04M
	c	With a neat diagram explain the Astable operation of IC 555 timer.	06M
MODULE 5			
9	a	Simplify the following Boolean expressions (i) $Y=A\acute{B}+AB$ (ii) $Y=AB+AC+BD+CD$ (iii) $Y=(B+CA)(C+\acute{A}B)$ (iv) $Y=\acute{A}\acute{B}\acute{C}\acute{D}+\acute{A}\acute{B}\acute{C}D+A\acute{B}\acute{C}\acute{D}+A\acute{B}\acute{C}D$	08M
	b	With a neat circuit diagram and truth table, explain the working of a JK flip flop.	06M

	c	With a neat diagram, explain the working of a communication system.	06M
		OR	
10	a	Simplify and realize the following using NAND gates only *(i)* $Y = AC + ABC + \acute{A}BC + AB + D$ *(ii)* $Y = A\acute{B}\acute{C} + \acute{A}\acute{B}\acute{C} + \acute{A}\acute{B} + \acute{A}\acute{C}$	08M
	b	With a neat circuit diagram and truth table, explain the full adder circuit.	06M
	c	With a neat block diagram, explain the operating principle of the GSM system.	06M

CBCS SCHEME

USN | | | | | | | | | | |

18ELN14/24

First/Second Semester B.E. Degree Examination, Dec.2019/Jan.2020
Basic Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the working of PN junction diode under forward and reverse biased conditions. **(06 Marks)**

b. Explain the working of Photodiode. **(05 Marks)**

c. Explain with neat circuit diagram and waveforms, the working of full wave bridge rectifier. Show that the efficiency of full wave bridge rectifier is 81%. **(09 Marks)**

OR

2 a. Explain the operation of Half wave rectifier with capacitor filter with neat circuit diagram and waveforms. **(06 Marks)**

b. A full wave rectifier uses 2 diodes having internal resistance of 10 Ω each. The transformer RMS secondary voltage from center to each end is 200V. Find I_m , I_{dc} , I_{rms} and V_{dc} if the load is 800 Ω. **(06 Marks)**

c. Explain how zener diode helps in voltage regulation with neat circuit diagram. Give detail mathematical analysis. **(08 Marks)**

Module-2

3 a. Explain the construction, working and characteristics of n-channel JFET. **(09 Marks)**

b. With a neat circuit diagram, explain the working of CMOS Inverter. **(06 Marks)**

c. For a n-channel JFET if $I_{DSS} = 9$ mA and $V_p = -6$V. Calculate I_D at $V_{gs} = -4$V and V_{gs} at $I_D = 3$ mA. **(05 Marks)**

OR

4 a. Explain the construction, working and characteristics of enhancement type MOSFET. **(09 Marks)**

b. Explain the working of Silicon Controlled Rectifier [SCR] using two transistor model. **(06 Marks)**

c. For an EMOSFET, determine the value of I_D if $I_{D(on)} = 4$ mA, $V_{gs(on)} = 6$V, $V_T = 4$V and $V_{gs} = 8$V. **(05 Marks)**

Module-3

5 a. What is an OP-AMP? List the characteristics of an ideal OP-AMP. **(06 Marks)**

b. Explain the operation of an OP-AMP as inverting amplifier with neat diagram and waveforms. **(06 Marks)**

c. Explain how OP-AMP can be used as (i) Integrator (ii) Voltage follower. **(08 Marks)**

OR

6 a. Explain the different input modes of an OP-AMP. **(06 Marks)**

b. Design an adder circuit using OP-AMP to obtain an output voltage, $V_o = -[2V_1 + 3V_2 + 5V_3]$. Assume $R_f = 10$ kΩ. **(06 Marks)**

c. Explain the following terms with respect to OP-AMP:
(i) CMRR (ii) Slew rate (iii) Input bias current (iv) Supply Voltage Rejection ratio. **(08 Marks)**

Module-4

7 a. With a neat circuit diagram, explain how transistor is used as an amplifier. Derive an equation for A_v. **(08 Marks)**
b. Explain RC phase shift oscillator with circuit diagram and necessary equations. **(08 Marks)**
c. Explain the voltage series feedback circuit and derive an equation for voltage gain, A_{vf}, with feedback. **(04 Marks)**

OR

8 a. With a neat circuit diagram, explain the working of Wein-bridge oscillator. **(08 Marks)**
b. Explain the operation of IC555 as an Astable oscillator with neat circuit diagram and necessary equations. **(08 Marks)**
c. The Transistor in CE configuration is shown in Fig.Q8(c) with RC = 1 kΩ and β_{DC} = 125. Determine
(i) V_{CE} at V_{in} = 0 V.
(ii) $I_{B(min)}$ to saturate the collector current
(iii) $R_{B(max)}$ when V_{in} = 8 V
$V_{CE(sat)}$ can be neglected.

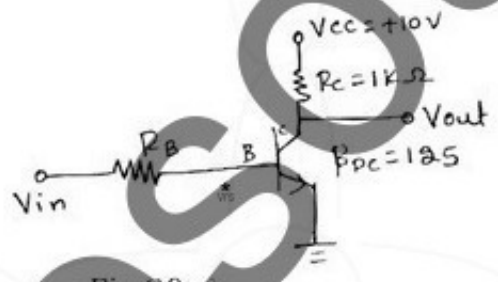

Fig.Q8(c) **(04 Marks)**

Module-5

9 a. Design Full adder circuit and implement it using basic gates. **(08 Marks)**
b. Find (i) $(1101\ 0111\ 0110\ 1010)_2 = (\ ?\ )_{16}$
(ii) $(EB986)_{16} = (\ ?\ )_2$
(iii) $(925.75)_{10} = (\ ?\ )_8$ **(06 Marks)**
c. Explain the basic elements of communication system with block diagram. **(06 Marks)**

OR

10 a. State and prove De-Morgan's theorem. **(06 Marks)**
b. With a block diagram, explain the working of a 3-bit ripple counter. **(06 Marks)**
c. What is a Flip-flop? Explain the operation of master-slave JK flip-flop. **(08 Marks)**

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B M S Institute Of Technology & Management

Dept Of Electronics and Communication Engineering

BATCH: 2020-21-ODD SEM: I Sem ECE A ,B AND C

SUBJCST: BASIC ELECTRONICS

Faculty In-Charge: Chandraprabha R/Dr. Surekha R. Gondkar/Dr. Vijayalakshmi G V

TARGET				LEVEL
60%	STUDENTS MUST SCORE	70%	& ABOVE	3-High
55%	STUDENTS MUST SCORE	70%	& ABOVE	2-Moderate
50%	STUDENTS MUST SCORE	70%	& ABOVE	1-Low

COURSE OUTCOMES	ATTAINMENT LVL-I A	ATTAINMENT LVL-UNIVERSITY	OVERALL ATTAINMENT LVL
CO1	3.00	0.00	1.8
CO2	0.00	0.00	0
CO3	0.00	0.00	0
CO4	0.00	0.00	0
CO5	3.00	0.00	1.8
CLASS STRENGTH	196		
SET TARGET	70%		

		TEST-1								TEST-2								TEST-3									CO1			CO2			CO3		
	CO No.	3	3	3	3	3	3	4	4	3	3	3	3	4	4	4	3	1	1	1	1	3	3	4	2	5	TOTAL	PERCENT		TOTAL	PERCENT		TOTAL	PERCENT	
	Question No.	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	ASSMT									
	MAXIMUM MARKS FOR QUESTION	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	20	X	Target >=70%	10	X	Target >=70%	70	X	
Sl No.	Name																																		
1	ANKIT SHARMA		10	9			7		9	4				9		2		9		5		6	9			10	11	55.00%	Y	5	50.00%		35	50.00%	
2	ASIF AYOUB BHATTI		8		10				9	2			1					9		9		6		4	2	10	10	50.00%	Y	2	20.00%		21	30.00%	
3	BHUVANA R		8		10		8	8	10	9		8	9				7	9		10		10		9	7	10	17	85.00%	Y	1	10.00%		55	78.57%	
4	LLOYD SWEEBERT LEWIS		10	6			8	7	7		10				8		8		10	9		9		10	9	10	15	75.00%	Y	5	50.00%		51	72.86%	
5	NEVAN GEORGE THOMAS		10	7		9		7	10		9	9			7		5	9		9			9	9	8	10	12	60.00%		8	80.00%	Y	33	51.43%	
6	SABANA N									10			9		9	2	8	9		9		9		9	9	10	18	90.00%	Y	5	50.00%		35	50.00%	
7	SPOORTHI M	9		6		10	9	9	9			9	9			9	7	8	9	6		9	9	9	9	10	21	105.00%	Y	2	20.00%		35	50.00%	
8	SUCHETHA P B									10		8		7		7	7	10		10	9		10	8	8	10	20	100.00%	Y	8	80.00%	Y	27	38.57%	
9	SVATHI G S									10		8		6		9	7		10			10		9	6	10	16	80.00%		6	60.00%		35	50.00%	
10	BARRAT	8		10			7	7	8		8		8	7			9	6		9		8			9	10	9	45.00%		5	50.00%		40	57.14%	
11	VIDHYA RAJ R		10	10		10		9	10		8			8	7	10	7		10	9		8		9	6	10	15	75.00%	Y	6	60.00%		43	61.43%	
12	UPEEN KUMAR M		10		10	8			8	8	9	9						7				7		10		10	7	35.00%		0	0.00%		47	67.14%	
13	DEEPAK DARSHAN P		9		10	7		8	9			9		8			8	7		9		8		7	8	10	16	80.00%	Y	4	40.00%		56	80.00%	
14	RAHUL VENKA									7		9				9		8		7		6		7	7	10	9	45.00%		1	10.00%		46	22.86%	
15	R SHREETA REDDY		10		9	7		9	8	7		8		8		9	8	9		9		10		9	9	10	18	90.00%	Y	9	90.00%	Y	51	72.86%	
16	MOHAMMED SADIB		10			9	8	9	9	9			9					8			8	8		8	8	9	12	60.00%		4	40.00%		36	51.43%	
17	PONNAM NAGA SRAVAN REDDY	9			9		9	9	9	9			9	8	8	9	9	9		9	9	10	9	8	8	10	8	40.00%		4	40.00%		43	61.43%	
18	VARSHA V									9	8	9			8		8									10	0	0.00%		0	0.00%		25	35.71%	
19	NIKHIL S		10	8		9		9	10									8		8		8	8	9	8	10	18	90.00%	Y	8	80.00%	Y	35	50.00%	
20	SURAJ S		9		10		9	9	9	9			8		9	9	9	9		9		9		9	9	10	18	90.00%	Y	2	20.00%		37	52.86%	
21	SNUBHAM		8		9	10		9	10		8	9		9		8	8	9		9		10		8	8	10	18	90.00%	Y	6	60.00%		47	67.14%	
22	D NARUN									8			8	7			9	7		8		8			9	10	11	55.00%		5	50.00%		35	50.00%	
23	TASMEEN TAJ N										9		7			8	9	9		10			9	10	8	10	15	75.00%		4	40.00%		29	41.43%	
24	PRADHANTH S		9		9	10			10		9			9	10		8	8		9		10		7	9	10	17	85.00%	Y	9	90.00%	Y	47	67.14%	
25	VINAYAKA REDDY B																																		

	TEST-1								TEST-2								TEST-3									CO1			CO2			CO3			
CO No.	3	3	3	3	3	3	4	4	3	3	3	3	4	4	4	3	1	1	1	1	3	3	4	2	5										
Question No.	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	ASSNI	TOTAL	PERCENT		TOTAL	PERCENT		TOTAL	PERCENT		TOTA
MAXIMUM MARKS FOR QUESTION	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	20	%	Target >=70%	10	%	Target >=70%	70	%	Target >=70%	40
Name																																			
ANIKET SHARMA		10	9			7		9	4				9		2		9		9		5		6	5	10	18	90.00%	Y	5	50.00%		35	50.00%		26
ASIF AYOUB BHATTI		8		10				9	2			1					9		9		6		4	2	10	18	90.00%	Y	2	20.00%		27	38.57%		13
BHUVAN A R		4		10		6	6	10	9		4	5				7	9		10		10		9	1	10	19	95.00%	Y	1	10.00%		55	78.57%	Y	25
LLOYD SWEEBERT LEWIS		10	6			8	7	7		10			8			8		10	9		9		10	5	10	19	95.00%	Y	5	50.00%		51	72.86%	Y	32
NEVAN GEORGE THOMAS		10	7		9		7	10		8	9			7		5	9		3			9	9	8	10	12	60.00%		8	80.00%	Y	57	81.43%	Y	33
SAHANA N									10			8		8	2	8	9		9		9		9	5	10	18	90.00%	Y	5	50.00%		35	50.00%		19
SPOORTHI M	5		6		10	3	0	5			3	2			2	1	8	4	9		5		9	2	10	21	105.00%	Y	2	20.00%		35	50.00%		16
SUCHETHA P B									10		6		7		1	1	10		10	5		10	8	8	10	25	125.00%	Y	8	80.00%	Y	27	38.57%		16
SWATHI G S									10		8		6		5	7		10			10		9	6	10	10	50.00%		6	60.00%		35	50.00%		20
TERENCE PRABHU BARRAT	4		10			7	7	8		8		4	1			3	6		3		4			5	10	9	45.00%		5	50.00%		40	57.14%		16
VISHVA RAJ R		10	10		10		5	10		8			8	7	10	1		10	9		4		3	6	10	19	95.00%	Y	6	60.00%		43	61.43%		43
LITESH KUMAR M		10		10	8			4	6	3	3						7				7		10		10	7	35.00%		0	0.00%		47	67.14%		14
DEEPAK DARSHAN P		9		10	7		0	5		5	9		4			8	7		9		8		7	4	10	16	80.00%	Y	4	40.00%		56	80.00%	Y	16
RAHUL VENK K									7		3			2			8		1		6		7	1	10	9	45.00%		1	10.00%		16	22.86%		9
R SHREEYA REDDY		10		9	7		5	8	7		4		8		3	4	9		9		10		5	9	10	18	90.00%	Y	9	90.00%	Y	51	72.86%	Y	29
MOHAMMED SAQIB		10			9	4	6	6	2			3					8			4	8		8	4	5	12	60.00%		4	40.00%		36	51.43%		20
PONNAM NAGA SRAVAN REDDY	5			6		6	6	9	3			3	4	4	1	7	7		1		10	3	8	4	10	8	40.00%		4	40.00%		43	61.43%		32
VARSHA V									7	4	6			8		8									10	0	0.00%		0	0.00%		25	35.71%		8
NIKHIL S		10	4		9		5	10									8		8		6	6	5	8	10	16	80.00%	Y	8	80.00%	Y	35	50.00%		20
SUHAS S		6		10		6	6	2	3			4		2	2	3	9		9		5		6	2	10	18	90.00%	Y	2	20.00%		37	52.86%		18
SHUBHAM		4		8	10		8	10		4	5		9		4	6	9		9		10		4	6	10	18	90.00%	Y	6	60.00%		47	67.14%		35
G THARUN									4			2	7			5	7		4		4			5	10	11	55.00%		5	50.00%		15	21.43%		7
YASMEEN TAJ H										5		7			4	9	9		10			8	10	4	10	19	95.00%	Y	4	40.00%		29	41.43%		14
PRASHANTH S		5		9	10			10		5			8	10		8	8		9		10		7	9	10	17	85.00%	Y	9	90.00%	Y	47	67.14%		35
VINAYAKA REDDY B KONDIKOPPA									5	2		7	2		2		9		9		7		9	4	10	18	90.00%	Y	4	40.00%		21	30.00%		13
SUBRAHMANYA LAKSHMI KESHAV BHUMARAJU									8		9		8		4	2									10	0	0.00%		0	0.00%		19	27.14%		12
IRENE MARIA DANIEL		10		4		10	6	10									9		9		9		8	9	10	18	90.00%	Y	9	90.00%	Y	33	47.14%		24
JAYANTH J										4	9		3		2	8									10	0	0.00%		0	0.00%		21	30.00%		5
ARCHANA B																									10	0	0.00%		0	0.00%		0	0.00%		0
SIMRAN GUPTA									9			5	3			2	9		9		10		8	4	10	18	90.00%	Y	4	40.00%		26	37.14%		11
MEGHANATHA REDDY P		10	9		5			4	10			7		4	5	5	9		2	4	10		4	1	10	15	75.00%	Y	1	10.00%		56	80.00%	Y	17
DEEKSHITHA B S		10	9			9	8	6	5.5		7			3.5	7	5	9		9			8	8	2	10	18	90.00%	Y	2	20.00%		53.5	76.43%	Y	32.5
ALLA VAMSI KRISHNA									7		6		7		5	6	7		9		10		9	4	10	16	80.00%	Y	4	40.00%		29	41.43%		21
LETI MANISH KUMAR		10	10			10	6	9	9.5		7.5		3		3		8		9		10		8	5	10	17	85.00%	Y	5	50.00%		57	81.43%	Y	29
ACHYUTHA GOWDA C P										5	8		10		4	6	9		6		9		3	7	10	15	75.00%	Y	7	70.00%	Y	28	40.00%		17
SHREYA G D									7		6		4		2	6		9	10		10		9	8	10	19	95.00%	Y	8	80.00%	Y	29	41.43%		15
ASHISH SRINIVASAN																		7	1		9		9	4	5	8	40.00%		4	40.00%		9	12.86%		9
YASHODHA S SHRIDHAR										1		4			3	2		6	2			7	8	2	10	8	40.00%		2	20.00%		14	20.00%		11
SHIVA KUMAR P		10	3	5	3			5	1	2		4				7	7	6	2		7		9	4	10	15	75.00%	Y	4	40.00%		42	60.00%		14
THEJASWINI H A		4	4			4		10	4		10			7	3	8	9		5		10		8	3	10	14	70.00%	Y	3	30.00%		44	62.86%		28
BHUVANA H	9	5			10	5	6	10		8	3				3	2	9		9		10		9	8	10	18	90.00%	Y	8	80.00%	Y	52	74.29%	Y	28
BHEEMIREDDY HARINI		8		4	10			10	8		5		6		4	2		6	2		9		5	4	10	8	40.00%		4	40.00%		46	65.71%		25
VANCHIREDDY DEEPIKA									5		6	3	4		3	4		9	4		8		9	4	10	13	65.00%		4	40.00%		26	37.14%		16
ABHAY SINGH		10	9			8	7	10		4		9	10			9	7		9		8		9	6	10	16	80.00%	Y	6	60.00%		57	81.43%	Y	36

	CO RESULT	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	
Understand the operation of semiconductor devices and circuits	3													1	1	
Apply the knowledge of basics of semiconductor devices to build electronic circuits.	3	3												1	1	
Analyze the working of analog and digital circuits for any application.	3		3											1	1	
Design electronic systems using analog and digital devices.	3			3					3	3	3		3	1	1	
Design and demonstrate(Hardware/simulation) the basic applications of electronic circuits	3				2	3			3	3	3		3	1	1	
SUM		3	3	3	2	3	0	0	6	6	6	0	6	5	5	
Ciii*		3	3	3	2	3	0	0	3	3	3	0	3	1	1	
		1	1	1	1	1	0	0	2	2	2	0	2	5	5	0

	CO RESULT	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	
Understand the operation of semiconductor devices and circuits	1.8	0	0	0	0	0	0	0	0	0	0	0	0	0.6	0.6	
Apply the knowledge of basics of semiconductor devices to build electronic circuits.	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Analyze the working of analog and digital circuits for any application.	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Design electronic systems using analog and digital devices.	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Design and demonstrate(Hardware/simulation) the basic applications of electronic circuits	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
SUM		0	0	0	0	0	0	0	0	0	0	0	0	0.6	0.6	
ATTAINMENT		0	0	0	0	0	0	0	1.8	1.8	1.8	0	1.8	0.6	0.12	

COURSE OUTCOMES	ATTAINMENT LVL-I A	ATTAINMENT LVL-UNIVERSITY	OVERALL ATTAINMENT LVL
CO1	3.00	0.00	1.8
CO2	0.00	0.00	0
CO3	0.00	0.00	0
CO4	0.00	0.00	0
CO5	3.00	0.00	1.8
CLASS STRENGTH	196		
SET TARGET	70%		

COURSE OUTCOMES	ATTAINMENT LVL-I A	ATTAINMENT LVL-UNIVERSITY	OVERALL ATTAINMENT LVL
CO1	3.00	0.00	1.8
CO2	0.00	0.00	0
CO3	0.00	0.00	0
CO4	1.00	0.00	0.6
CO5	3.00	0.00	1.8
CLASS STRENGTH	196		
SET TARGET	60%		