BMS INSTITUTE OF TECHNOLOGY & MANAGEMENT

(An Autonomous institution affiliated to VTU, Belagavi)
Doddaballapur Main Road, Avalahalli, Yelahanka, Bengaluru- 560119

Department of Electronics and Communication Engineering

M. Tech. – VLSI System Design

Scheme (I-IV Semesters)
and
Syllabus (Semester I)

Academic Year: 2025 - 26

Approved by BoS on 09.08.2025

Institute Vision

To emerge as one of the finest technical institutions of higher learning, to develop engineering professionals who are technically competent, ethical and environment friendly for betterment of the society.

Institute Mission

Accomplish stimulating learning environment through high quality academic instruction, innovation and industry-institute interface.

Department Vision

Be a pioneer in providing quality education in electronics, communication, and allied engineering fields to serve as a valuable resource for industry and society

Department Mission

1. To nurture students with a strong foundation in theoretical and practical concepts through innovative pedagogy and industry interface.
2. To foster interdisciplinary research, entrepreneurship skills and instill professional ethics by providing experiential learning opportunities.

Program Educational Objectives (PEOs):

1. Excel in professional career, lead research in the area of VLSI and allied fields.
2. Exhibit professional ethics, effective communication and teamwork in solving engineering problems by adapting industry standards for sustainable development of society.

Program Outcomes (POs):

PO1: An ability to Apply the knowledge of Mathematics, Science and Engineering to solve VLSI Design problems

PO2: An ability to Analyse and design complex VLSI circuits, using suitable analytical methods, Electronic Design Automation (EDA) tools.

PO3: An ability to independently carry out research /investigation and development work to solve practical problems

PO4: An ability to write and present a substantial technical report/document

PO5: An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

Scheme (I-IV semester)

M.Tech.- VLSI System Design (VSD)

BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

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Scheme of Teaching and Examinations – 2025 Scheme

Outcome-Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2025 – 26 onwards)

I Semester M.Tech. VLSI System Design

Sl. No.	Course Category	Course Code	Course Name	Teaching Department	Credits Distribution				Examination				Contact Hours/week
					L	T	P	Total	CIE Marks	SEE Marks	Total Marks	SEE Duration (H)	
1	PCC	MVSD101	ASIC design	EC	3	0	0	3	50	50	100	3	3
2	IPCC	MVSD102	Digital System Design (Lab will be on FPGA)	EC	3	0	1	4	50	50	100	3	5
3	PCC	MVSD103	Digital IC Design	EC	3	0	0	3	50	50	100	3	3
4	PEC	MVSD104X	Professional Elective-I	EC	3	0	0	3	50	50	100	3	3
5	PEC	MVSD105X	Professional Elective-II	EC	3	0	0	3	50	50	100	3	3
6	PCCL	MVSDL106	Digital IC Design lab	EC	0	0	2	2	50	50	100	3	4
7	NCMC	MRMI107	Research Methodology and IPR	-	-	-	-	-	Online courses (online.vtu.ac.in)				
TOTAL					**15**	**0**	**3**	**18**	**300**	**300**	**600**		

Professional Elective-I		**Professional Elective-II**	
Course Code	**Course Title**	**Course Code**	**Course Title**
MVSD104A	Static Timing Analysis	MVSD105A	Scripting for VLSI
MVSD104B	On-Chip Communication Architectures	MSVD105B	Advanced Computer Architecture
MVSD104C	RISC-V Architecture and Design	MSVD105C	VLSI Process Technology
MVSD104D	Physics of VLSI Devices	MSVD105D	Micro and Nano devices

Note: PCC: Professional core. **IPCC**- Integrated Professional Core Courses, **PCCL-**Professional Core Course lab, **NCMC**- None Credit Mandatory Course, **L-** Lecture, **P-**Practical, **T/SDA**- Tutorial / Skill Development Activities(Hours are for Interaction between faculty and students), **MRMI107-** Research Methodology and IPR **(Online)** for the students who have **not studied** this course in the Undergraduate level. This course is not counted for vertical progression, Students have to qualify for the award of the master's degree.

PCC: Professional Core Course: Courses related to the stream of engineering, which will have both CIE and SEE components, students have to qualify in the course for the award of the degree. **Integrated Professional Core Course (IPCC)**: Refers to a Professional Theory Core Course Integrated with practical of the same course. The IPCC's theory part shall be evaluated by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper.

PCCL: Professional Core Course Laboratory: Practical courses whose CIE will be evaluated by the class teacher and SEE will be evaluated by the two examiners.

Skill development activities: Under Skill development activities in a concerning course, the students should

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.

Gain confidence in the modeling of systems and algorithms for transient and steady-state operations, thermal study, etc. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s are to be involved either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities that will enhance their skills. The prepared report shall be evaluated for CIE marks.

MRMI107-Research Methodology and IPR- None Credit Mandatory Course (NCMC) if students have not studied this course in their undergraduate program then he /she has to take this course at http://online.vtu.ac.in and to qualify for this course is compulsory before completion of the minimum duration of the program (Two years), however, this course will not be considered for vertical progression.

MVSD- M.Tech VLSI System Design

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II Semester M.Tech. VLSI System Design

Sl. No.	Course Category	Course Code	Course Name	Teaching Department	Credits Distribution				Examination				Contact Hours/week
					L	T	P	Total	CIE Marks	SEE Marks	Total Marks	SEE Duration (H)	
1	IPCC	MVSD201	Physical Design	EC	3	0	1	4	50	50	100	3	5
2	PCC	MVSD202	Analog IC Design	EC	4	0	0	4	50	50	100	3	4
3	PCC	MVSD203	VLSI Testing	EC	3	0	0	3	50	50	100	3	3
4	PCC	MVSD204	System Verilog for Verification	EC	3	0	0	3	50	50	100	3	3
5	PEC	MVSD205X	Professional Elective-III	EC	3	0	0	3	50	50	100	3	3
6	PEC	MVSD206X	Professional Elective-IV	EC	3	0	0	3	50	50	100	3	3
7	PCCL	MVSDL207	Analog IC Design Lab	EC	0	0	1	1	50	50	100	3	3
8	AEC	MVSD208	VLSI Testing and Verification Lab	EC	0	0	1	1	50	50	100	3	2
TOTAL					**19**	**0**	**3**	**22**	**400**	**400**	**800**	-	-

Professional Elective-III		Professional Elective-IV	
Course Code	**Course Title**	**Course Code**	**Course Title**
MVSD205A	Mixed Signal IC Design	MVSD206A	System on Chip
MVSD205B	RF IC Design	MVSD206B	Low Power VLSI Design
MVSD205C	VLSI Digital Signal Processing	MVSD206C	Bio-Medical CMOS ICs
MVSD205D	High Performance Computing Architectures	MVSD206D	CAD for VLSI

Note: **PCC**: Professional core. **IPCC**-Integrated Professional Core Courses, **PCC(PB):** Professional Core Courses (Project Based), **PCCL**-Professional Core Course lab**, PEC-** Professional Elective Courses, **MDC-** Multi-Disciplinary Courses , **L-Lecture, P-Practical, T/SDA-Tutorial / Skill Development Activities** (Hours are for Interaction between faculty and students),**L-Lecture, P-Practical, T-Tutorial** (Hours are for Interaction between faculty and students).
Note: **MVSD** means specialization code for example **M.Tech . in VLSI System Design.**

Ability Enhancement Courses (AEC):. These courses are designed to help students enhance their skills in communication, language, and personality development. They also promote a deeper understanding of subjects like social sciences and ethics, culture and human behavior, human rights, and the law.

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III Semester M. Tech. VLSI System Design

Sl. No.	Course Category	Course Code	Course Name	Teaching Department	Credits Distribution				Examination				Contact Hours/ week
					L	T	P	Total	CIE Marks	SEE Marks	Total Marks	SEE Duration (H)	
1	PCC	MVSD301	NPTEL Online Course (12 weeks duration)	EC	3	0	0	3	--	100	100	-	
2	PCC	MVSD302	NPTEL Online Course (12 weeks duration)	EC	3	0	0	3	--	100	100	-	
3	PCC	MVSD303	NPTEL Online Course (12 weeks duration)	EC	3	0	0	3	--	100	100	-	
4	INT	MVSDI304	Internship Phase I (Research/Industry Internship)	EC	0	0	5	5	100	--	100	-	10
5	PW	MVSDP305	Project Phase I	EC	0	0	4	4	100	--	100	-	8
TOTAL					**9**	**0**	**9**	**18**	**200**	**300**	**500**		**18**

- **Professional Core Course (PCC):** It is an Online course and been proctored by the faculty throughout the semester. Students can choose the online course/certification programs from NPTEL (The courses are identified by BOS). They may present the final certificate for internal assessment. Student can take the course during II semester break and need to submit the course completion certificate before semester end examination for evaluation.
- **Internship Phase-I:** All the students shall have to undergo mandatory internship of 4-6 weeks during the semester. Those, who have not pursued /completed the internship, shall be declared as fail in internship course and have to complete the same during subsequent semester end examinations after satisfying the internship requirements.
- **Project Work Phase-I:** Students in consultation with the guide/co-guide if any shall pursue literature survey and complete the preliminary requirements of selected Project work. Each student shall prepare relevant introductory project document and present a seminar. CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded for project work phase -1 shall be based on the evaluation of Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25.

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IV Semester M.Tech. VLSI System Design

Sl. No.	Course Category	Course Code	Course Name	Teaching Department	Credits Distribution				Examination				Contact Hours/ week
					L	T	P	Total	CIE Marks	SEE Marks	Total Marks	SEE Duration(H)	
1	INT	MVSDI401	Internship Phase II (Research/Industry Internship)	EC	0	0	10	10	100	100	200	3	20
2	PW	MVSDP402	Project Phase II	EC	0	0	12	12	100	100	200	3	24
TOTAL					**0**	**0**	**22**	**22**	**200**	**200**	**400**	**-**	**44**

- **Internship Phase-II:** All the students shall have to undergo mandatory internship of 6-8 weeks during the semester. Those, who have not pursued /completed the internship, shall be declared as fail in internship course and have to complete the same during subsequent semester end examinations after satisfying the internship requirements.
- **Project Work Phase-II:** CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any, and a senior faculty of the department. The CIE marks awarded for project work phase -2 shall be based on the evaluation of Project Report subjected to plagiarism check, Project Presentation skill and Question and Answer session in the ratio 50:25:25. SEE shall be at the end of IV semester. Project work evaluation and Viva-Voce examination (SEE), after satisfying the plagiarism check (below 20%).

Syllabus (I semester)

M.Tech.- VLSI System Design (VSD)

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – I

ASIC Design (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD101**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Learn the ASIC methodologies and programmable logic cells to implement a function on IC.
2. Understand the issues and tools related to ASIC design and implementation
3. Acquire the knowledge of physical design and partitioning methods
4. Summarize the floor planning, placement and routing techniques

Module – 1

Introduction to ASICs:
Types of ASICs: Full Custom ASICs, Standard Cell based ASICs, Gate array based ASICs, Channelled gate array, Channel less gate array, structured gate array, Programmable logic devices, Field Programmable Gate Arrays, Design Flow,
Data logic cells: Data Path Elements, Adders, Multipliers, Arithmetic operator (Practical approach), I/O Cell, Cell Compilers. (8 Hours)

Module – 2

ASIC Library Design:
Logical effort: Predicting delay, logical area and logical efficiency, logical paths, multistage cells, optimum delay, optimum no. of stages. Library cell design.
Programmable ASICS: The Antifuse, Static RAM, EPROM and EEPROM technology (8 Hours)

Module – 3

Programmable ASICs logic cells:
Xilinx LCA: XC3000 CLB, XC4000 Logic Block, XC5200 Logic Block, Xilinx CLB Analysis.
Programmable ASIC Design Software: Design System, logic synthesis, Introduction to Synthesis and Simulation.
Low- Level Design Entry: Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC'S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation. (8 Hours)

Module – 4

ASIC Construction:
Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, Power dissipation, FPGA partitioning.
Partitioning methods: partitioning example, Constructive Partitioning, Iterative Partitioning Improvement, Kernighan algorithm, The ratio-cut algorithm, Look Ahead algorithms. (8 Hours)

Module – 5

Floor Planning and Placement & Routing:
Floor planning: Floor planning goals, Floor planning tools, I/O and power planning, clock planning. **Placement:** Placement goals, algorithms, iterative placement improvement, Time driven placement methods. Physical Design flow.
Routing: Global Routing goals and methods, Detail Routing, Left edge algorithm, Area routing algorithm, Special Routing, Circuit Extraction and DRC. (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Appreciate the types of ASICs, VLSI design flow and data logic cells.

CO2: Analyze the design parameters for speed, area, power optimization and FPGA programming technologies for design of ASICs

CO3: Apply the features of logic cells, FPGA design flow and design entry required for ASIC design

CO4: Analyze the importance of system partitioning and its methods in the physical design

CO5: Apply the back-end physical design flow, including floor planning, placement and Routing techniques for digital system design.

Suggested Learning Resources:

Text Books:

1. M J S Smith, Application -Specific Integrated circuits, Pearson Education, Seventh impression 2010.

References:

1. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, ISBN: 978-1-4614-1119-2. 2011
2. Rakesh Chadha, Bhasker J, "An ASIC Low Power Primer", Springer, ISBN:978-14614-4270-7.

Web Resources:

1. https://onlinecourses.nptel.ac.in/noc24_ee77/preview.
2. https://www.scribd.com/document/482509792/ASIC-Lab

M.TECH. VLSI System Design
Choice-Based Credit System (CBCS)
Semester – I

Digital System Design (3:0:1) 4
(Effective from the academic year 2025-26)

Course Code	**MVSD102**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:2	SEE Marks	50
Total Number of Contact Hours	40 Hrs + 10 Lab sessions	Exam Hours	3

Course Objectives:

This course will enable students to:

1. To introduce digital system design using Verilog HDL.
2. To understand synthesis and design optimization for FPGAs.
3. To explore FPGA architectures and programmable logic devices.
4. To design processor subsystems and system-level architectures.

Module – 1

Introduction and Methodology: Digital systems and embedded systems, Binary representation and circuit elements, Real-world circuits, Models, Design methodology

Combinational Basics: Boolean Functions, Boolean Algebra, Verilog Models of Boolean Equations, Using Vectors for Binary Codes, Bit Errors, Decoders and Encoders, Multiplexers, Active-Low Logic (8 Hours)

Module – 2

Number Basics: Unsigned integers, Coding Unsigned Integers, Operations on Unsigned Integers, signed integers, Coding signed Integers, Operations on signed Integers, Fixed and floating-point numbers (8 Hours)

Module – 3

Sequential Basics: Storage elements, Counters, Sequential data paths and control, finite state machines, Clocked synchronous timing methodology (8 Hours)

Module – 4

Memories: Concepts, Memory types, Asynchronous static RAM, Synchronous Static RAM, Dynamic RAM Read-Only Memories, Error detection and correction (8 Hours)

Module – 5

Introduction to Verilog: Structure of Verilog module, Operators, Data Types, Styles of Description.

Verilog Data flow description: Highlights of Data flow description, Structure of Data flow description.

Verilog Behavioral description: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers

Verilog Structural description: Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder. (8 Hours)

	PRACTICAL COMPONENT OF IPCC
Sl.NO	**Verilog code design, simulate and synthesize the following with a suitable FPGA**
1	Verilog implementation of 8:1 Mux/Demux.
2	Verilog implementation of 8 to 3 programmable priority Encoder
3	Verilog implementation of Full Adder using structural modeling
4	Verilog implementation of 8-bit ripple carry adder, carry skip adder.

5	Verilog implementation of Flip Flops (D, SR, T, JK)	
6	Verilog implementation of 4-bit shift register (SISO, SIPO, PISO)	
7	Verilog implementation of 4-bit binary up/down/up-down counter with synchronous reset, BCD counter	
8	Sequence generator/detectors, synchronous FSM-Mealy and Moore machine.	

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Apply the concepts of number system and digital circuit logic to design digital systems using Verilog.
2. Apply the basics of sequential circuits, including storage elements and finite state machines, to design simple clocked digital systems using Verilog.
3. Analyze the operations of different memory structures and also error detection, correction methods.
4. Design combinational and sequential logic circuits using Verilog constructs at the RTL level.

Suggested Learning Resources:

Text Books:

1. Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", Elesvier, 2010.
2. HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dream tech press.
3. Bruno, Frank. FPGA Programming for Beginners. Packt Publishing, 2021.

References:

1. Digital Systems Design Using Verilog, 1st Edition, 2015, Charles Roth, Lizy K. John, ByeongKil Lee, Cengage Learning, ISBN-10: 1285051076
2. Digital Design using Verilog, Elsevier, 2007, W. Wolf 5. Stuart S, Simon David & Peter Flake "System Verilog for Design" A guide to using System Verilog for Hardware design and modelling, Springer publication, 2nd Edition, 2006.

Web Resources:

1. https://freevideolectures.com/course/2319/digital-systems-design
2. http://www.asicguru.com/system-verilog/tutorial/introduction/1
3. https://www.chipverify.com/systemverilog/systemverilog-tutorial
4. https://nptel.ac.in/courses/106/108/106108099/
5. https://nptel.ac.in/courses/117/106/117106092/
6. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-111 introductory-digital-systems-laboratory-spring-2006/index.htm

M.Tech. in VLSI System Design
Choice Based Credit System (CBCS)
SEMESTER - I

Digital IC Design (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD103**	CIE Marks	50
Teaching Hours/Week (L:T:P)	3:0:0	SEE Marks	50
Total Number of Lecture Hours	40	Exam Hours	03

Course objectives:

This course will enable students to

1. Learn CMOS process technology Realize digital circuits using different MOS and CMOS techniques
2. Acquire the knowledge of different digital subsystems
3. Analyze different CMOS circuits
4. Design Combinational and sequential Circuits

Module – 1

Basic MOS technology:
Integrated circuits era. Enhancement and depletion mode MOS transistors. nMOS fabrication. CMOS fabrication. Twin tub process, Bi-CMOS technology.

MOS Transistor Theory:
Introduction, MOS Device Design Equations, The Complementary CMOS Inverter- ideal I-V and CV characteristics, Switch level RC delay models. Noise Margin. The Differential Inverter, Transmission Gate (8 Hours)

Module – 2

Performance estimation of static and dynamic CMOS Designs:
CMOS Complementary Logic, Bi CMOS Logic, Pseudo-nMOS Logic, Dynamic CMOS Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS Domino Logic, Cascaded Voltage Switch Logic (CV)

Circuit Design Processes:
MOS layers. Stick diagrams. Design rules and layout – lambda-based design and other rules. Examples. Layout diagrams. Basic Physical Design of Simple logic gates. (8 Hours)

Module – 3

Delay: Introduction, ,Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths, Input Ordering Delay Effect, Skewed Gates (8 Hours)

Module – 4

Sequential Circuit Design : Sequencing Static circuits, Circuit Design of Latches and flip flops, Conventional CMOS Latches, Conventional CMOS Flip flops, Pulsed Latches, Resettable latches and flip flops. (8 Hours)

Module – 5

Memory Designs and array Structures:
Memory Classification, Memory Architectures and building blocks. The memory core; Read Only Memories (ROM), Non Volatile Read-Write memories, Random Access Memories (RAM). Content Addressable Memories (CAM) Cells designs, Case studies in Memory designs.

(8 Hours)

Course Outcomes: The students will be able to:

- CO1: Apply the CMOS technology concepts in realizing different logical structures
- CO2: Analyse different CMOS circuits
- CO3: Design layouts for different digital structures
- CO4: Design Combinational Circuits and Sequential circuits
- CO5: Evaluate the performance of digital Systems/subsystems using modern tools.

Textbooks

1. N.H. Weste and David Harris**,** "CMOS VLSI Design – A Circuits and Systems Perspective"**,** 2015**,** Fourth Edition , Pearson.
2. Jan M Rabaey, Anatha chandrakasana, Nikolic, Digital integrated circuits, A design Perspective, 2016, second edition, PHI.

References

1. R. Jacob Baker, "CMOS Circuit Design, Layout and Simulation", John Wiley India Pvt. Ltd, 2008
2. Sung- Mo Kang & Yusuf Leblebici **,** "CMOS Digital Integrated Circuits", Analysis and Design , 3rd Edition, Tata McGrawHill Publishing Company Ltd., New Delhi, 2007.
3. A Hodges, H.G Jackson and R.A Saleh. , Analysis and Design of Digital Integrated Circuits, 3rd Edition, Tata McGraw-Hill Publishing Company Limited, New Delhi. 2007.

Web Resources:

1. https://www.youtube.com/playlist?list=PL1w8k37X_6L92ySuv9B0Fg1rMiL1OE1_1
2. https://nptel.ac.in/courses/117106092
3. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-374-analysis-and-design-of-digital-integrated-circuits-fall-2003

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – II

Static Timing Analysis (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD104A**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand the concepts of delays, timing parameters, and clock behaviour in digital circuits.
2. Explore STA flow resources such as libraries, netlists, parasitics, and constraints for delay estimation.
3. Analyse the impact of noise, crosstalk, and parasitic effects on circuit timing in nanometer designs.
4. Apply STA constraints, recognize timing exceptions, and identify/fix violations such as setup and hold using STA tools.

Module – 1

Introduction: Introduction, timing analysis of digital circuits, Sequential Elements in RTL.
Delay Concepts for Digital Designing: Types of Delays in Digital Circuits, Different Cause for Delay
Timing parameters of digital circuits: Timing Parameters for Combinational Logic Gates, Timing Parameters for Sequential Circuits, Concept of Delay Path in a Design, Clock Concepts. (8 Hours)

Module – 2

Resources for Static Timing Analysis Flow: Libraries, Netlist, Parasitics for Delay Calculation: Device Parasitic, Interconnects, Parasitic Extraction formats, constraints for design, Back annotation. (8 Hours)

Module – 3

Concepts of Noise and Crosstalk for static timing Analysis: Coupling Capacitance Concept, Cross talk, Type of Crosstalk Noise or Glitch, Types of Crosstalk Delta Delay, Noise Libraries, Crosstalk Effect on Timing Analysis, Strategy of Crosstalk on Nanometre Design. (8 Hours)

Module – 4

Constraints for STA: Clock Constraints, Other Timing Constraints, External Delays of DUA, Timing Exceptions: Multicycle Path, False Path, Clock Grouping, Case Analysis, Disable Timing, Path with Derate (8 Hours)

Module – 5

Timing Violations and Verification: Slack, Critical Path of Timing Report, Setup Violation, Hold Violation, Multicycle Path, Half Cycle Path, Timing Checks for Asynchronous Timing Paths, Input / Output Timing Path Checks, DRC Violation Check, Multi Speed Clock Domain, Crosstalk Checks, Techniques to Fix Timing Violation: Techniques to Fix Setup Violations, Techniques to Fix Hold Violations. (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Apply timing concepts and delay parameters to analyze combinational and sequential circuits.

CO2: Apply libraries, netlists, and parasitic models in STA flow for delay estimation.

CO3: Analyse the impact of noise and crosstalk on circuit timing and suggest mitigation methods.

CO4: Examine the timing constraints, exceptions and their effect on circuit behaviour.

CO5: Analyse timing violations using STA reports and recommend effective fixes for design closure.

Suggested Learning Resources:

Text Books:

1. Static Timing Analysis for VLSI circuits", R. Jayagowri, Pushpendra S. Yadav, MEDTECH, A Division of Scientific International, 2020.

References:

1. "Static Timing Analysis for Nanometer Designs: A Practical Approach", J. Bhasker, R. Chadha, Springer, 2009.

Web Resources:

1. https://nptel.ac.in/courses/106/102/106102181/ NOC: synthesis of digital systems.

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – I

On-Chip Communication Architectures (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD104B**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand on chip communication architecture.
2. Explore different standards of on chip communication architecture.
3. Summarize the scocket based and off chip bus interface standards .
4. Explain the models for performance, power and thermal estimation.

Module – 1

Introduction: Trends in System on chip design, ESL design flow, On-chip communication architecture.

Bus based communication architecture: Terminology, characteristics of bus based communication architecture, data transfer modes, bus topology types, physical implementation of bus wires. (8 Hours)

Module – 2

On-Chip communication architecture standards: Amba 2.0, Amba 3.0, IBM core connect, sonics smart interconnect. (8 Hours)

Module – 3

Communication architecture standards : Altera Avalon, Avalon-ST.

Socket-based On-Chip Bus Interface Standards: Open core protocol, OCP Profiles, VSIA Virtual Component Interface**,** Philips Device Transaction Level Protocol, off-chip bus architecture standards. (8 Hours)

Module – 4

Models for Performance Exploration: Static performance estimation models, Dynamic (simulation-based) performance estimation models, hybrid communication architecture performance estimation approaches. (8 Hours)

Module – 5

Introduction To NoC: OSI layer rules in NoC - Interconnection Networks in Network-on-Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support. (Text 2) (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Summarize architecture, data transfer models and types of bus wires,.
CO2: Apply knowledge of Amba 2.0, 3.0 and standards for interconnection on chip architecture hardware.
CO3: Use socket based and off chip standards for interconnection of components on the chip.
CO4: Analyze the static, dynamic and hybrid system performance models on chip architecture.
CO5: Explore the techniques required for the construction of network on chip.

Suggested Learning Resources:

Text Books:

1. Sudeep Pasricha, Nikil Dutt, " On-Chip Communication Architectures ", Morgan Kaufmann is an imprint of Elsevier.2008
2. SantanuKundu, Santanu Chattopadhyay "Network-on-Chip: The Next Generation of System on-Chip Integration",2014 CRC Press

References:

1. Frank Bruno,"FPGA Programming for Beginners", Packt Publishing Ltd, 2021
2. Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R.Das" Networks-on - Chip , Architectures Holistic Design Exploration", Springer

Web Resources:

1. https://nptel.ac.in/courses/106103183
2. https://elearn.nptel.ac.in/shop/partnering-courses/registration-ongoing/advanced-arm-socs-design-batch-3/?v=c86ee0d9d7ed

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – I

RISC-V Architecture and Design (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD104C**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand the RISC-V ISA and its design philosophy.
2. Develop assembly-level programming skills using RISC-V.
3. Design and implement RISC-V-based microprocessor cores.
4. Explore privilege levels, interrupts, CSRs, and memory protection.
5. Integrate RISC-V core with SoC components and test on FPGA/simulators.

Module – 1

Introduction to RISC-V Architecture: Evolution of Instruction Set Architectures (ISAs): RISC vs CISC, Introduction to RISC-V: Modular open-source ISA, Base ISA RV32I, RV64I: instruction formats (R, I, S, B, U, J), RISC-V Assembly Language Programming basics, - Register conventions, toolchains, and simulators (Venus, Ripes). (8 Hours)

Module – 2

Instruction Set Extensions and Programming : Arithmetic and logical operations, Load/store and control transfer instructions, RISC-V M-extension (Multiplication/Division), Pseudo-instructions and optimization, Compressed extension (RVC) overview, Assembly programming practices using simulators. (8 Hours)

Module – 3

Microarchitecture and CPU Design: Single-cycle and pipelined processor design, Datapath and control unit architecture, Instruction execution stages: IF, ID, EX, MEM, WB, Hazards: data, control, and structural, Branch prediction and pipelining strategies, RTL implementation overview in Verilog. (8 Hours)

Module – 4

Privilege Architecture, Traps, and CSRs: RISC-V privilege levels: User, Supervisor, Machine, Exception and interrupt handling, Control and Status Registers (CSRs): definitions and access, Physical Memory Protection (PMP), Basic MMU features and address translation, Trap vector configuration and delegation. (8 Hours)

Module – 5

SoC Integration and Open-source Ecosystem: RISC-V-based SoC design: buses (AXI, AHB), peripherals (UART, Timer), Open-source RISC-V cores: PicoRV32, Rocket Chip, VexRiscv, FPGA prototyping of RISC-V SoC, Introduction to LiteX, Freedom Studio, and VexRiscv , Case studies: RISC-V in commercial and academic projects, Emerging extensions: RISC-V Vector, Security, AI (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Explain the principles and advantages of RISC-V architecture

CO2: Write assembly-level programs using RISC-V instruction sets.

CO3: Design and simulate a RISC-V-based pipelined processor.

CO4: Analyze the role of privilege levels, interrupts, and CSR registers.

CO5: Demonstrate integration of RISC-V cores into SoC platforms using FPGA.

Suggested Learning Resources:

Text Books:

1. David Patterson and Andrew Waterman, The RISC-V Reader: An Open Architecture Atlas, 1st Edition, Strawberry Canyon LLC, 2017.
2. David A. Patterson and John L. Hennessy, Computer Organization and Design RISC-V Edition: The Hardware Software Interface, 2nd Edition, Morgan Kaufmann, 2020.

References:

1. SiFive and RISC-V Foundation Documentation – https://riscv.org/technical/specifications
2. Krste Asanovic et al., The RISC-V Instruction Set Manual: Volume I: User-Level ISA
3. Tutorials and documentation from GitHub repositories for RISC-V cores (e.g., PicoRV32, RocketChip)

Web Resources:

1. https://riscv.org
2. https://github.com/mortbopet/Ripes (RISC-V simulator)
3. https://riscv.org/learn/education/
4. https://riscv.org/technical/specifications/

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – I

Physics of VLSI devices (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD104D**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Explain basics of semiconductor physics and electronic devices
2. Explain physics and modelling of PN-Junction, MOS Capacitors and MOSFETs
3. Understand and discuss various short channel effects and issues in deep sub-micron MOSFETs
4. Understand physics of multi-gate transistors

Module – 1

Review of fundamentals: Energy bands, Metals, Semiconductors and Insulators, Electrons and Holes

Semiconductors: Direct and Indirect semiconductors, Intrinsic and Extrinsic materials, Density of states, Fermi distribution, Free carrier densities, Boltzmann statistics, Conductivity and Mobility, Drift and Resistance, Effects of temperature and doping on mobility.

Current flow mechanisms: Drift current, diffusion current, mobility of carriers, current density equation, and continuity equation. (8 Hours)

Module – 2

PN Junctions: Thermal equilibrium physics- Energy band diagrams, space charge layers, Poisson equation, electric fields and potential, p-n Junction under applied bias.

Static current-voltage characteristics, Reverse bias breakdown: Zener breakdown, avalanche breakdown. (8 Hours)

Module – 3

MOS Capacitor: The Ideal MOS capacitor: Accumulation, depletion and strong inversion regions, threshold voltage, Gate work function, Oxide and Interface charges, Body effect, C-V characteristics of MOS at low and high frequency. (8 Hours)

Module – 4

MOSFETs and Compact Models: The MOSFET structure, working principle and drain characteristics, threshold voltage of MOSFET, MOSFET modelling with SPICE Level 1, 2, 3 for above threshold region, subthreshold Characteristics, Effect of gate and drain voltage on carrier mobility in inversion region.

Scaling and Short Channel Effects: Constant electric field and constant power supply scaling, Effect of scaling – Channel length modulation, Punch through, hot carrier degradation, drain induced barrier lowering. (8 Hours)

Module – 5

Modern MOSFET Principles/Quantum Effects and Advanced MOSFET Structures: Classical Mechanics and its drawbacks, Quantum mechanics, 1D problem – particle in a box, electron tunneling., Non-uniform doping in a channel, High-k dielectrics, Deep submicron devices, structure and basic principle of operation: Double & trigate SOIMOSFETs, and FINFETs, Buried Channel MOSFET. (8 Hours)

Course outcomes :

At the end of the course, the student will be able to:

CO1: Understand the band structure and diagrams of semiconductors

CO2: Design the extrinsic semiconductors with specific carrier concentration and model the carrier transport mechanism in semiconductors

CO3: Design of PN – Junction for given specifications

CO4: Understand the physics of MOS capacitors, MOSFETs and spice level models

CO5: Understand short channel effects of MOSFETs and deep submicron devices.

CO6: Understand the basics of multi-gate transistors to mitigate short channel effects.

Suggested Learning Resources:

Text Books:

1. Ben G Streetman and S Banerjee, Solid State Electronic Devices, 7th Edition Pearson 2018
2. Donald A Neamen, Dhrubes Biswas, Semiconductor Physics and Devices, Mc Grew Hill.
3. Nandita Das Gupta and Amitava Das Gupta, Semiconductor Devices: Modelling and Technology, Printice Hall of India,

References:

1. Y P Tsividis and Colin McAndrew, Operation and Modelling of the MOS Transistor, 2011, Third Edition, Oxford University Press, U. S
2. Introduction to Semiconductor Materials and Devices by M. S. Tyagi, John Wiley & Sons, 5th Edition,2005
3. J. P. Colinge and C. A Colinge, Physics of Semiconductor Devices, 2017, Kluwer Academic Publishers U. S.
4. J. P. Colinge, FinFETs and other multi-gate Transistors, 2020, Springer
5. V. Mitin, V. Kochelap, M. Stroscio, Introduction to Nanoelectronics, Cambridge University press, 2008
6. Rainer Waser, Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices, Wiley-VCH, 2003

Web Resources:

1. https://www.youtube.com/watch?v=QQ6Wr5VC3bA

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – I

Scripting for VLSI (3:0:0) 3
(Effective from the academic year 2025-26)

Course Code	**MVSD105A**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. To write scripts in the LINUX environment.
2. To study the principles of Scripting Languages like Perl, TCL and Python.
3. To write the scripts for automation using the languages like Perl, TCL and Python.

Module – 1

LINUX Basics : Introduction to Linux, File System of Linux, General usage of Linux Kernel and Basic Commands, Linux users and group, Permissions for file, directory and users, Searching a file and directory, zipping and unzipping concepts. (8 Hours)

Module – 2

PERL Basics : History and Concepts of PERL, Scalar Data, Arrays and List Data, Control structures, Hashes, Basics I/O,Regular Expressions, Functions, Miscellaneous control structures, Formats. (8 Hours)

Module – 3

Advanced Topics in PERL: Directory access, File and Directory manipulation, Process management, Packages and Modules -Applications of PERL scripts to Electronic Design Automation. (8 Hours)

Module – 4

TCL basics: An Overview of TCL and Tk, Tcl Language syntax, Variables, Expressions, Lists, Control flow, procedures, Errors and exceptions, String manipulations. (8 Hours)

Module – 5

Python Basics: Introduction to Python, Using Python interpreter, Brief tour on standard library, Control flow Tools, Data structures, Regular Expressions, Classes, Modules, Applications, Python scripts to Electronic Design Automation (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Explain and apply commands in LINUX environment.
CO2: Develop and execute the Perl scripts.
CO3: Analyze and Handle files, directories and manage processes using Perl scripts.
CO4: Use TCL scripts for automation and Build TCL scripts to Handle files, directories and manage process.
CO5: Develop Python scripts to interpret files and directories.

Suggested Learning Resources:

Text Books:

1. Larry Wall, Tom Christiansen, John Orwant, Programming PERL, 2012, Fourth Edition, Oreilly Publications.
2. John K, Ousterhout, Ken Jones, Tcl and the Tk Toolkit, 2010, Second Edition, Pearson Education, India

References:

1. Guido van Rossum Fred L. Drake, Jr., editor, Python Tutorial Release 3.2.3, 2012, Python Software Foundation.
2. Randal L. Schwartz, Brian D Foy, Tom Phoenix, Learning Perl, 2021, 8th Edition, O'Reilly Media, Inc.
3. Mark Lutz, Learning Python, 2013, 5th Edition, O'Reilly Media, Inc.

Web Resources:

1. https://onlinecourses.nptel.ac.in/noc24_ee134/preview
2. https://nptel.ac.in/courses/106106182

M.TECH. VLSI System Design

Choice Based Credit System (CBCS)

Semester – I

Advanced Computer Architecture (3:0:0) 3

(Effective from the academic year 2025-26)

Course Code	**MVSD105B**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

- Understand the concepts of parallel processing and its applications.
- Analyze the performance of different scalar computers.
- Develop pipelining techniques for efficient instruction execution.
- Explore memory hierarchy and cache design for performance optimization.
- Implement hardware for arithmetic operations.
- Discuss instruction set architecture design and its impact on processor efficiency.

Module – 1

Multiprocessors and multi-computers, Multi-vector and SIMD computers, Vector and SIMD Supercomputers, PRAM and VLSI Models, Conditions of Parallelism, Hardware and Software parallelism. (8 Hours)

Module – 2

Advanced processor technology: CISC and RISC Scalar Processor, Memory hierarchy technology, Cache memory organization: Cache Addressing Models, Shared memory organization. (8 Hours)

Module – 3

Linear pipeline processors, Non-linear pipeline processors: Reservation and Latency Analysis, Instruction pipeline design: Instruction Execution Phases, Mechanisms for Instruction Pipelining, Arithmetic design, Superscalar pipeline design. (8 Hours)

Module – 4

Vector Processing principle, Multi-vector multiprocessors, Compound Vector processing, Principles of multithreading, Fine grain multicomputer, Scalable and multithread architectures, Dataflow and hybrid architectures. (8 Hours)

Module – 5

Parallel programming models, Parallel languages and compilers, Parallel programming environments, Synchronization and multiprocessing modes, Message passing program development: Synchronous and Asynchronous Message Passing. (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Apply the basic knowledge of partitioning and scheduling in Multiprocessors.

CO2: Analyze cache memory, virtual memory and shared memory organizations.

CO3: Analyze the design properties of Linear and Non - Linear processors.

CO4: Apply the principles of multithreading in hybrid Architectures.

CO5: Write any parallel programming models for various architectures and Applications.

Suggested Learning Resources:

Text Books:

1. K. Hwang, “Advanced Computer Architecture”, Tata McGraw Hill, 3rd Edition, 2018.
2. W. Stallings, “Computer Organization and Architecture”, McMillan, 11th edition, 2022.

References:

1. Hennessy, John L., and David A. Patterson. Computer architecture: a quantitative approach. Elsevier, 2012, 5th Edition.
2. M.J. Quinn, “Designing Efficient Algorithms for Parallel Computer”, McGraw Hill, 1994.

Web Resources:

1. Advanced Computer Architecture: https://onlinecourses.nptel.ac.in/noc23_cs07/preview
2. Advanced Computer Architecture: https://www.cse.iitb.ac.in/~biswa/courses/CS683/main.html

M.TECH. VLSI System Design

Choice Based Credit System (CBCS)

Semester – I

VLSI Process Technology (3:0:0) 3

(Effective from the academic year 2025-26)

Course Code	**MSVD105C**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. To understand the principles of semiconductor device fabrication.
2. To study various fabrication processes and technologies used in modern VLSI chip manufacturing.
3. To provide knowledge on photolithography, oxidation, doping, etching, deposition, and metallization.
4. To comprehend the challenges and advances in nanometer process technologies.

Module – 1

Introduction to IC Process Technology : Introduction to IC fabrication and cleanroom concepts, Wafer preparation: Crystal growth, slicing, lapping, polishing, Cleanroom classifications, contamination sources and control, Basic steps in IC fabrication: Overview of CMOS flow, Moore's Law and scaling trends (8 Hours)

Module – 2

Oxidation and Diffusion: Thermal oxidation: Dry and wet oxidation, kinetics, Deal-Grove model, Oxide growth systems and characteristics, Dopant diffusion: Fick's laws, diffusion profiles, Ion implantation: Mechanism, dose, energy, range, Annealing and activation (8 Hours)

Module – 3

Photolithography and Etching: Photolithography: Photoresists (positive & negative), exposure methods, Contact, proximity, and projection printing, Resolution enhancement techniques (RET), Etching: Wet and dry etching, plasma and reactive ion etching (RIE), Etch selectivity, anisotropy, etch rate control (8 Hours)

Module – 4

Thin Film Deposition and Metallization: CVD (Chemical Vapor Deposition): LPCVD, PECVD, APCVD, PVD (Physical Vapor Deposition): Sputtering, evaporation, Dielectric films: SiO_2, Si_3N_4, High-k materials, Metallization: Aluminum, Copper, barrier layers, Electromigration, reliability, and contact formation (8 Hours)

Module – 5

Process Integration and Advanced Technologies: CMOS process integration: Well formation, isolation, gate stack, silicides, LOCOS, STI, LDD, Spacer techniques, Process challenges at sub-10nm nodes, FinFET, SOI, 2.5D, 3D IC process considerations, Reliability and yield analysis. (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Analyze different steps in IC fabrication and cleanroom protocols.

CO2: Explain thermal oxidation and diffusion mechanisms in VLSI process flow.

CO3: Illustrate photolithographic patterning and etching techniques.

CO4: Evaluate thin film deposition and metallization processes.

CO5: Discuss advanced process technologies and integration challenges.

Suggested Learning Resources:

Text Books:

1. S.M. Sze and Kwok K. Ng, VLSI Technology, 2nd Edition, McGraw Hill, 2003.
2. S.K. Ghandhi, VLSI Fabrication Principles – Silicon and Gallium Arsenide, Wiley, 2nd Edition, 2008.

References:

1. Simon M. Sze, Semiconductor Devices – Physics and Technology, Wiley, 2008.
2. James Plummer, Michael Deal, Peter Griffin, Silicon VLSI Technology: Fundamentals, Practice, and Modeling, Pearson, 2nd Edition.
3. Stephen A. Campbell, Fabrication Engineering at the Micro and Nanoscale, Oxford University Press, 2013.

Web Resources:

1. https://nptel.ac.in/courses/117107127
2. https://ocw.mit.edu/courses/6-152j-micro-nano-processing-technology-fall-2005/

M.TECH. VLSI System Design
Choice Based Credit System (CBCS)
Semester – I

Micro and Nano devices (3:0:0)3
(Effective from the academic year 2025-26)

Course Code	**MSVD105D**	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Number of Contact Hours	40	Exam Hours	3

Course Objectives:

This course will enable students to:

1. Understand the fundamentals of microscale and nanoscale devices used in VLSI systems.
2. Analyze the physics, materials, and scaling limits of semiconductor devices.
3. Explore the design, fabrication, and applications of MEMS and NEMS-based systems.
4. Understand emerging device concepts beyond CMOS and their integration challenges.
5. Learn nano-fabrication techniques and their role in future electronic device technologies.

Module – 1

Introduction to Micro and Nano Devices: Overview of micro/nano device applications in VLSI systems. Semiconductor fundamentals, quantum confinement, density of states, scaling theory. Introduction to MOSFET scaling, short-channel effects. (8 Hours)

Module – 2

MEMS and NEMS Devices: Working principles and structures of MEMS (Micro-Electro-Mechanical Systems) and NEMS (Nano-Electro-Mechanical Systems). Mechanical and electrical transducers: piezoelectric, capacitive, and thermal actuation. (8 Hours)

Module – 3

Nanoelectronic Devices and Materials: Carbon Nanotubes (CNTs), Nanowires, and Quantum Dots. Device physics of CNT-FETs, FinFETs, TFETs, and Spintronic devices. Role of 2D materials (graphene, MoS_2) in nanoelectronics. (8 Hours)

Module – 4

Fabrication Techniques for Micro/Nano Devices: Top-down and bottom-up fabrication. Photolithography, E-beam lithography, Atomic Layer Deposition (ALD), Molecular Beam Epitaxy (MBE), Etching (Dry and Wet). (8 Hours)

Module – 5

Emerging Technologies and Applications: Beyond-CMOS technologies: Tunnel FETs, Negative Capacitance FETs, Memristors, and Neuromorphic Devices. Device-circuit co-design issues. Reliability, variability, and packaging of nano devices. (8 Hours)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Understand the principles of micro and nano device physics and scaling behavior
CO2: Analyze the working of MEMS and NEMS devices and integration with VLSI platforms.
CO3: Apply knowledge of nano materials and device concepts for emerging electronic applications.
CO4: Understand the fabrication process flow and challenges in micro/nano manufacturing.
CO5: Evaluate next-generation device technologies and their application in futuristic electronics.

Suggested Learning Resources:

Text Books:

1. Mark Lundstrom, "Fundamentals of Nanotransistors", World Scientific Publishing, 2013.

2. Tai-Ran Hsu, "MEMS and Microsystems: Design and Manufacture", McGraw-Hill, 2002.

References:

1. George W. Hanson, "Fundamentals of Nanoelectronics", Pearson Education, 2008.
2. Bharat Bhushan (Ed.), "Springer Handbook of Nanotechnology", Springer, 2017.
3. Karl Goser, Jan Dienstuhl, "Nanoelectronics and Nanosystems", Springer, 2004.

Web Resources:

1. NPTEL Course on Nanoelectronics
2. MEMS/NEMS Introduction by MIT

M.Tech. in VLSI System Design
Choice Based Credit System (CBCS)
SEMESTER - I

Digital IC Design LAB (0:0.5:1.5) 2
(Effective from the academic year 2021-22)

Course Code	**MVSDL106**	CIE Marks	50
Teaching Hours/Week (L:T:P)	0:1:3	SEE Marks	50
Total Number of Lecture Hours	30	Exam Hours	03

Course objectives:

This course will enable students to

1. To explain the VLSI Design Methodologies using VLSI design tool.
2. To grasp the significance of various design logic Circuits in full-custom IC Design.
3. To explain the Physical Verification in Layout Extraction.
4. To fully appreciate the design and analyze of CMOS Digital Circuits.
5. To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

List of Experiments:

The students are required to design and implement the Circuit, calculate delay, Layout, RC extraction and Post layout simulation of experiments using CMOS Technology.

1. Inverter Characteristics.
2. NAND
3. Full Adder
4. 2:1 Multiplexer
5. D-Flip Flop
6. Synchronous/Asynchronous Counter

Open Ended Experiments

1. SR- Flip Flop
2. Asynchronous Counter
3. Static RAM Cell
4. Dynamic Logic Circuits
5. Linear Feedback Shift Register