BMS EDUCATION TRUST (R)
BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

YELAHANKA, BENGALORE-560064

(An Autonomous Institute, affilated to VTU, Belagavi; Approved by AICTE, New Delhi;
7 Programs Accredited by NBA; NAAC Accredited with 'A' grade)

Department of Electronics & Telecommunication Engineering (ETE)

OPEN COURSE/SKILL DEVELOPMENT PROGRAM

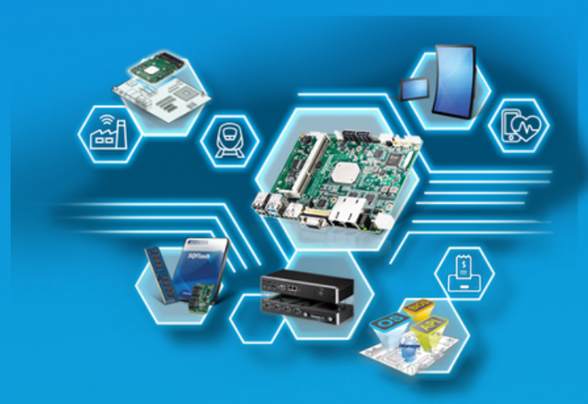
ON

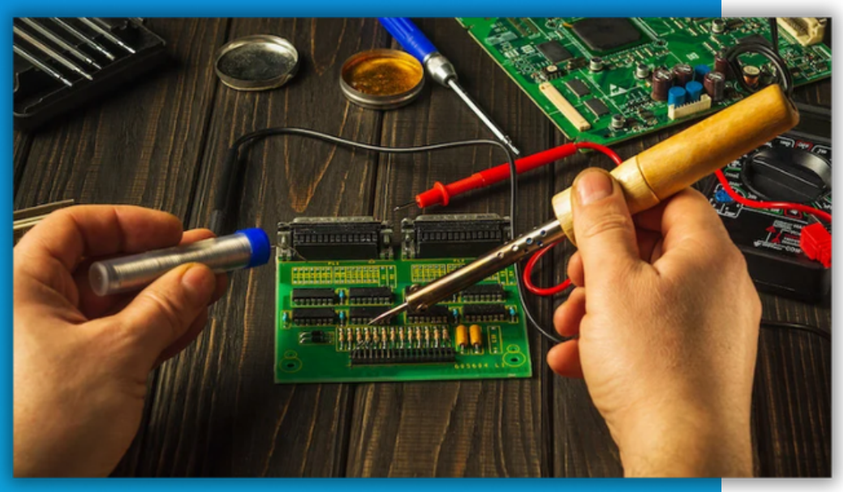
EMBEDDED SYSTEM DESIGN ON FPGAs

TRAINING BY INDUSTRY EXPERTS

12th-16th June 2023

Dept. of ETE, BMSIT&M Yelahanka, Bengaluru-64





Open to students from all streams of Engineering

COURSE CONTENTS

- INTRODUCTION TO FPGA ARCHITECTURE
- GPIO DESIGN
- SEQUENTAIL CIRCUITS,FSM DESIGN
- SDRAM MEMORY INTERFACING
- RTL DESIGN CONCEPTS
- DEBUGGING WITH ILA

REGISTRATION FEE is Rs.400/-

PAYMENT MODE

ONLINE

1.LOGIN INTO:HTTPS://BMSITM.GNUMS.IN
2.GO TO MENU - FEE-> OTHER FEE
3.SELECT THE FEE HEAD AS OPEN COURSE FEE AND PAY RS.400/-

RESOURCE PERSON'S

Mr. Nikil Rao
System Architect, VLSI & Embedded Domain
Dr. Prabhakar Mishra
Industry Consultant, Eminent Professor

COORDINATOR
Dr Sumathi M S
Assistant Prof. ETE Dept. BMSIT&M

Technical Support
Mrs Geetha N
Instructor

Department of Electronics & Telecommunication Engineering

Course Schedule: "Embedded System Design on FPGAs"

12th June 2023 to 16th June 2023

Sl No.	Date	Topics covered 8:30 to 10:30 am		Topics covered 10:50 to 12:50 pm		Topics covered 2:00 to 4:00 pm (4:00 pm to 4:30 pm-Assessment/feedback)
1	12.06.2023	**INAUGURATION,** FPGA Architecture Programmable Logic Devices, Programmable Read Only Memories	10:30 to 10:50 am TEA BREAK	Programmable Logic Arrays, Programmable Array Logic, Mux based Designs	12:50 to 1:50 pm LUNCH BREAK	GPIO (General Purpose I/O) design examples with verification using on-board LEDs and switches
2	13.06.2023	Sequential circuits, Finite State Machine design,		Reconfigurable Architectures		General Purpose I/O design example (using a 7-segment display
3	14.06.2023	FPGA Design flow – Design entry, Synthesis,		Synthesis for timing, placement and routing, STA.		Implementation SDRAM Memory interfacing
4	15.06.2023	RTL Design concepts, Clock Domain Crossing,		Debugging methods		Debugging with Integrated Logic Analyzer (ILA)
5	16.06.2023	Simulation of designs with inbuilt Quartus/Modelsim Intel FPGA edition		Implementation of UART/I2C		Valedictory

Instructions to the Participants:

1.Prerequisite: Students should have basic knowledge about Digital Electronics.

2.Students need to carry laptop.