ADDITIONAL OPEN ELECTIVES-B OFFERED BY EC/TC BOARD

B. E. EC/TE Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER – VII			
ARM EMBEDDED SYSTEMS			
Course Code	**18EC753**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40(8Hours/Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course objective: This course will enable students to:

- Understand the importance and applications of ARM Design
- Know the architecture of ARM processor
- Use instruction sets of ARM processor
- Analyze the adaptation of C code, firmware, OS, Interrupts, caches, etc. in ARM embedded systems

Module-1	RBT Level
ARM Embedded Systems Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications. **ARM Processor Fundamentals** ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions.	**L1, L2**
Module-2	
Introduction to the ARM Instruction set Introduction, Data processing instructions, Load - Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, Conditional Execution. ALP programming.	**L1, L2, L3**
Module-3	
Introduction to the THUMB instruction set Introduction, THUMB register usage, ARM – THUMB interworking, Other branch instructions, Data processing instructions, Stack instructions, Software interrupt instructions. ALP programming	**L1, L2, L3**
Module-4	
Efficient C Programming: Overview of C Compilers and optimization, Basic C data types, Local Variable Types, Portability issues **Exception and Interrupt Handling:** Exception Handling-ARM Processor Exceptions and Modes, Vector Table, Exception Priorities, Link Register Offset, Interrupts- Interrupt Latency, Basic Interrupt Stack design and implementation, Interrupt Handling Schemes (**general description only** of the schemes)	**L1, L2, L3, L4**
Module-5	
Firmware: Firmware and Bootloader **Embedded Operating Systems:** Fundamental Components **Caches:** The memory Hierarchy and caches memory-caches and memory management units, Cache architecture basic architecture of caches memory, basic operation of cache controller, the relationship between cache and main memory.	**L1, L2**

Course Outcomes: After studying this course, students will be able to:

1. Depict the organization, architecture, bus technology, memory and operation of the ARM processors
2. Employ the knowledge of Instruction set of ARM processors to develop basic Assembly Language Programs
3. Recognize the importance of the Thumb mode of operation of ARM processors
4. Describe the techniques involved in writing C code for ARM processors and Exception & Interrupt handling in ARM Processors
5. Describe the importance and use of Firmware, OS and cache in ARM Embedded systems

Students have to conduct the following experiments as a part of CIE marks along with other Activities:

Conduct the following experiments by writing Assembly Language Program (ALP) using ARM Cortex M3 Registers using an evaluation simulator and the required software tool.

1. Write an ALP to find the sum of 10 integer numbers.
2. Write an ALP to multiply two 16-bit binary numbers.
3. Write an ALP to find factorial of a number.
4. Write an ALP to add an array of 16-bit numbers and store the 32-bit result in internal RAM
5. Write an ALP to find the square of a number (1 to 10) using look-up table.
6. Write an ALP to find the largest/smallest number in an array of 32 numbers.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

"ARM System Developers Guide", Andrew N Sloss, Dominic System and Chris Wright, Elsevier, Morgan Kaufmann publisher, 1st Edition, 2008, ISBN:1758608745.

References:

1. "ARM System on chip Architecture", Furber S, Addison Wiley, 2nd Edition, 2008, ISBN:9780201675191
2. "Embedded System", Rajkamal, Tata McGraw-Hill Publishers, 2nd Edition, 2008, ISBN: 0070494703.