



BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

(Autonomous Under VTU) Yelahanka – Bengaluru – 560119

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech. I SEMESTER TIMETABLE FOR THE ACADEMIC YEAR 2025- 26 (ODD Semester)

W.E.F-03.11.2025

Semester: I

Branch : ECE/PG/-VLSI System Design (VSD)

PG Coordinator: Dr. Banuprakash R

Class Room: VLSI Lab (III Floor)

	08.30 -09.25	09.25 -10.20	10.20 -10.40	10.40 - 11.35	11.35 - 12.30	12.30- 01.25	01.25 - 02.20	02.20 - 03.15	03.15 - 04.10
MON	←--DSD IPCC lab (SR & BR)----→		SHORT BREAK	AD (BR)	DSD (SR)	LUNCH BREAK	Proctoring		
TUE	PE-II-ACA (LS)	STA (JKB)		DSD (SR)	DID (RH)		Club Activity		
WED	AD (BR)	PE-II-ACA (LS)		DID (RH)	STA (JKB)		*Bridge Course (Linux)		
THUR	STA (JKB)	DSD (SR)		AD (BR)	DID (RH)				
FRI	←-----Digital IC Design lab (JKB & BR)-----→				PE-II-ACA (LS)				
SAT									

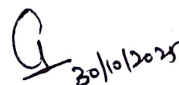
*Bridge Course Classes (10 hours)

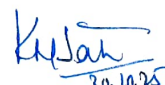
COURSE	COURSE CODE	CREDITS	COURSE COORDINATOR
ASIC design	MVSD101	3	Dr. Banuprakash R
Digital System Design (Lab will be on FPGA)	MVSD102	4	Dr. Sabina Rahaman
Digital System Design IPCC lab			Dr. Sabina Rahaman & Dr. Banuprakash R
Digital IC Design	MVSD103	3	Dr. Raju Hajare
Professional Elective-I (Static Timing Analysis)	MVSD104A	3	Dr. Jagannath K B
Professional Elective-II (Advanced Computer Architecture)	MVSD105B	3	Dr. Laxmi Sagar H S
Digital IC Design lab	MVSDL106	2	Dr. Jagannath K B & Dr. Banuprakash R
Research Methodology and IPR	MRMI107	--	Online Course

Note: First and Third Saturdays of the month are holidays.


Time Table Officers


HOD


Chief TTO


Dean Academics


Principal