BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT

(Autonomous Under VTU) Yelahanka – Bengaluru– 560119

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MTech. II SEMESTER TIMETABLE FOR THE ACADEMIC YEAR 2025– 26 (EVEN Semester)

W.E.F–23/03/2026 to 22/07/2026

Semester: II
Branch : ECE/PG/-VLSI System Design (VSD)

PG Coordinator: Dr. Banuprakash R
Class Room: VLSI Lab (III Floor)

	08. 30 –09. 25	09. 25 –10. 20	10.20 –10.40	10.40 – 11.35	11.35 – 12.30	12.30– 01.25	01.25 – 02. 20	02.20 – 03.15	03.15 – 04.10
MON	PD	SV		VT	AD		←--------PD Lab (JKB/SR) ---------→		
TUE	AD	PE-III		SV	PE-IV		←---Analog ICD Lab (SR/RH)------→		
WED	PE-III	AD	SHORT BREAK	PD	VT	LUNCH BREAK			
THUR	PD	SV		PE-IV	AD				
FRI	PE-IV	VT		PE-III	Proctoring		←-VLSI T&V Lab (VU/JKB/PC)---→		
SAT									

*Bridge Course classes conducted for 10 hours.

COURSE	COURSE CODE	CREDITS	COURSE COORDINATOR
Physical Design	MVSD201	4	Dr. Banuprakash R (IPCC LAB – JKB/SR)
Analog IC Design	MVSD202	4	Dr. Sabina Rahaman
VLSI Testing	MVSD203	3	Mr. Vivekananda U
System Verilog for Verification	MVSD204	3	Dr. Jagannath K B
Professional Elective-III	MVSD205X	3	Dr. Raju Hajare
Professional Elective-IV	MVSD206X	3	Dr. Jayadeva G S
Analog IC Design Lab	MVSDL207	1	Dr. Sabina Rahaman/ Dr. Raju Hajare
VLSI Testing and Verification Lab	MVSD208	1	Mr. Vivekananda U/Dr. Jagannath K B/Mr. Pinaki Chakraborty

Note: First and Third Saturdays of the month are holidays. Professor of Practice Mr. Pinaki Chakraborty will handle VLSI Testing and Verification Theory and laboratory.

Time Table Officers   HOD   Chief TTO   Dean Academics   Principal